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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte TAO HONG and MARKUS THOBEN¹

Appeal 2015-001693
Application 13/163,200
Technology Center 2800

Before MICHAEL J. STRAUSS, DANIEL N. FISHMAN, and
JAMES W. DEJMEK, *Administrative Patent Judges*.

Opinion for the Board filed by FISHMAN, *Administrative Patent Judge*.

Opinion concurring filed by DEJMEK, *Administrative Patent Judge*.

DECISION ON APPEAL

Appellants appeal under 35 U.S.C. § 134(a) from a Final Rejection of claims 1–20.² We have jurisdiction over the pending claims under 35 U.S.C. § 6(b).

¹ Appellants identify INFINEON TECHNOLOGIES AG as the real party in interest. Appeal Brief 2.

² In this Decision, we refer to Appellants' Appeal Brief ("App. Br.," filed June 19, 2014); Appellants' Reply Brief ("Reply Br.," filed October 24, 2014); the Final Office Action ("Final Act.," mailed January 9, 2014); the Examiner's Answer ("Ans.," mailed on August 25, 2014); and the original Specification ("Spec.," filed June 17, 2011).

We reverse.

THE INVENTION

Appellants' invention is directed to "resistance measurement by means of a shunt resistor." Spec. ¶ 2.

Independent claim 1, reproduced below, is representative:

1. A circuit arrangement with a populated circuit carrier, comprising:

a flat insulation carrier having a top side and a patterned metallization layer on the top side;

a first power semiconductor chip arranged on a first section of the metallization layer, the first power semiconductor chip having a first lower chip load terminal electrically conductively connected to the first section;

a shunt resistor arranged on a second section of the metallization layer, the shunt resistor having a lower main terminal electrically conductively connected to the second section; and

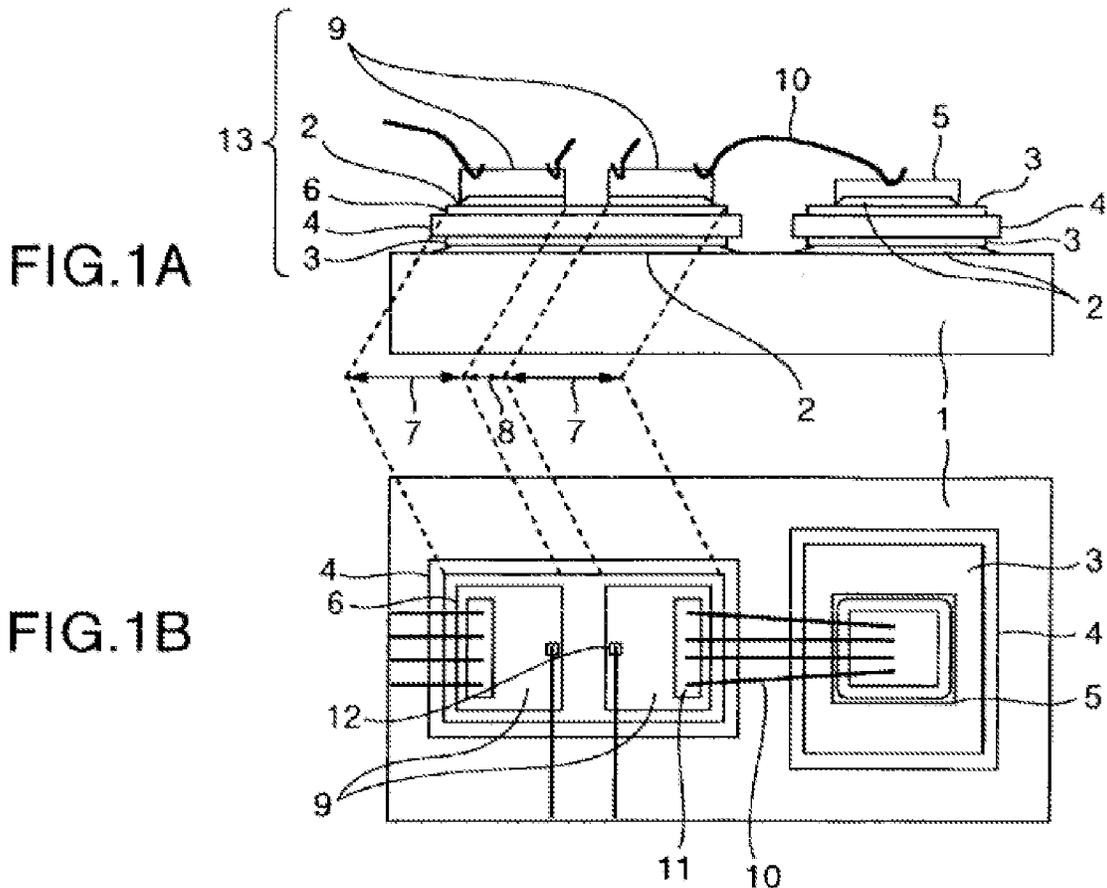
an electrically conductive connection between the first section and the second section, the electrically conductive connection having a constriction of the metallization layer between the first section and the second section so that a current which flows between the first lower chip load terminal and the lower main terminal during operation of the circuit arrangement must pass through the constriction.

THE REJECTION

Claims 1–20 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Nakatsu et al. (US 2003/0090241 A1; May 15, 2003) ("Nakatsu") and Chan et al. (US 5,451,818; Sept. 19, 1995) ("Chan").
Final Act. 2–14.

ANALYSIS

The Examiner and Appellants principally disagree regarding the proper interpretation of “semiconductor chip” as recited in claim 1 and as similarly recited in claim 17. The Examiner finds the recited first power semiconductor chip in the teachings of Nakatsu as “comprising 5, 10, 11, wherein electrode 11 is an extension of semiconductor switching device 5 through 10.” Final Act. 3 (citing Nakatsu Fig. 1B). Nakatsu’s Figures 1A and 1B are reproduced below.



Figures 1A and 1B of Nakatsu depict a side view and a top view, respectively, of switching device 5 coupled to electrode 11 via aluminum wire 10.

Appellants argue, “Nakatsu’s aluminum wire 10 and plate main electrode 11 are *not* considered as integral components of a ‘first power semiconductor chip’.” App. Br. 10. Appellants point to paragraph 48 of their Specification as defining “semiconductor chip.” *Id.* (“The first power semiconductor chip 1 is a vertical power semiconductor component comprising a semiconductor body 10, which is provided with a lower load terminal 11 and with an upper load terminal 12.”). In particular, we agree with Appellants that “[t]he only element of Nakatsu’s arrangement that can be plausibly considered a ‘semiconductor chip,’ within the meaning of the claims, is Nakatsu’s switching device 5.” *Id.* at 12.

Appellants and the Examiner both refer to dictionaries to support their respective interpretations of “semiconductor chip.” *See* App. Br. 11, 17–18; Ans. 4–6. Our reviewing court has recently summarized appropriate sources used in claim construction as follows:

The words of a claim are generally given their ordinary and customary meaning, which is the meaning that the term would have to a person of ordinary skill in the art at the time of the invention. Claim language must be viewed in light of the specification, which is the “single best guide to the meaning of a disputed term.” In accordance with *Phillips*, we first look to the actual words of the claims and then read them in view of the specification. Although courts are permitted to consider extrinsic evidence (e.g., expert testimony, dictionaries, treatises), such evidence is generally of less significance than the intrinsic record. Extrinsic evidence may not be used “to contradict claim meaning that is unambiguous in light of the intrinsic evidence.” “The construction that stays true to the claim language and most naturally aligns with the patent’s description of the invention will be, in the end, the correct construction.”

Profectus Tech. LLC v. Huawei Techs. Co., 823 F.3d 1375, 1380–81 (Fed. Cir. 2016) (internal citations omitted).

In general, the Examiner relies on a dictionary definition (originally cited by Appellants), stating “Merriam-Webster defines ‘chip’ in terms of integrated circuits, and Merriam-Webster defines ‘integrated circuits’ as: ‘a tiny complex of electronic components **and their connections** that is produced in or on a small slice of material (as silicon).” Ans. 4. Based on this definition, the Examiner concludes, “one of ordinary skill in the art, giving the terms their plain meaning[,] would include device 5 and connections 10 and 11 as disclosing the claimed ‘power semiconductor chip.’” *Id.*

We disagree with the Examiner. Nakatsu’s aluminum wire 10 and plate main electrode 11 do not represent components of a discrete semiconductor body as asserted by Appellants reliance on paragraph 48 of the Specification. Thus, the Examiner’s interpretation based on extrinsic evidence is inconsistent with the Specification (intrinsic evidence).

Furthermore, considering the Examiner’s proposed dictionary definition, the *connections* associated with an integrated circuit are necessarily “in or on a small slice of material (as silicon).” *Id.* Wire 10 and electrode 11 of Nakatsu do not appear to meet this definition. To the contrary, the Examiner’s definition from Merriam-Webster supports Appellants’ proposed definition based on paragraph 48 of the Specification—namely, the connections of a semiconductor chip (i.e., an integrated circuit) must be formed in or on the substrate (e.g., silicon slice).

Therefore, we conclude Nakatsu’s aluminum wire 10 and plate main electrode 11 are *not* properly considered components of the claimed first power *semiconductor chip* when the term is properly construed in accord with the Specification. Therefore, we agree with Appellants that “[i]f one

considers *only* the switching device 5 of Nakatsu as corresponding to the claimed first power semiconductor chip, . . . [then] switching device 5 is not *arranged on* . . . a metallization that electrically connects the switching device 5 to any part of the shunt resistor 13.” Thus, the proposed combination does not meet the claimed limitation of a semiconductor chip. App. Br. 9–10.

Appellants raise additional issues in the Briefs regarding the rejection of claim 1. We are persuaded of error with regard to the identified issue discussed *supra*, which is dispositive as to the rejection of all claims. Therefore, we do not reach the additional issues.

For the reasons discussed *supra*, and on the record before us, we are constrained to reverse the Examiner’s rejection of independent claim 1. For similar reasons, we do not sustain the Examiner’s rejection of independent claim 17, which recites similar limitations. Additionally, we do not sustain the Examiner’s rejection of dependent claims 2–16 and 18–20.

DECISION

We reverse the Examiner’s decision to reject claims 1–20.

REVERSED

Appeal 2015-001693
Application 13/163,200

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Before MICHAEL J. STRAUSS, DANIEL N. FISHMAN, and
JAMES W. DEJMEK, *Administrative Patent Judges*.

DEJMEK, *Administrative Patent Judge*, Concurring.

Although I concur with the Majority in reversing the Examiner's decision to reject claims 1–20 under 35 U.S.C. § 103(a), I write separately because, although I agree the Examiner erred in finding the combination of Nakatsu's switching device (5), electrode (11), and wire (10) corresponds to Appellants' claimed first power semiconductor chip, I do not find this error fatal to the Examiner's rejection.

Appellants' claimed invention is directed to a circuit arrangement including a shunt resistor to allow for a precise current measurement. Spec. ¶ 7. In a disclosed embodiment, the circuit arrangement comprises a flat insulation carrier having a patterned metallization layer on top. Spec. ¶ 8. A semiconductor chip is electrically conductively connected to a first section of the metallization layer and a shunt resistor is electrically conductively

connected to a second section of the metallization layer. Spec. ¶ 8. Further, “[a]n electrically conductive connection is provided between the first section and second section” allowing current to flow between the terminal of the semiconductor chip electrically conductively coupled to the first section of the metallization layer and the terminal of the shunt resistor electrically conductively coupled to the second section of the metallization layer. Spec. ¶ 8.

Figure 2A from Appellants’ Specification is illustrative and is reproduced below:

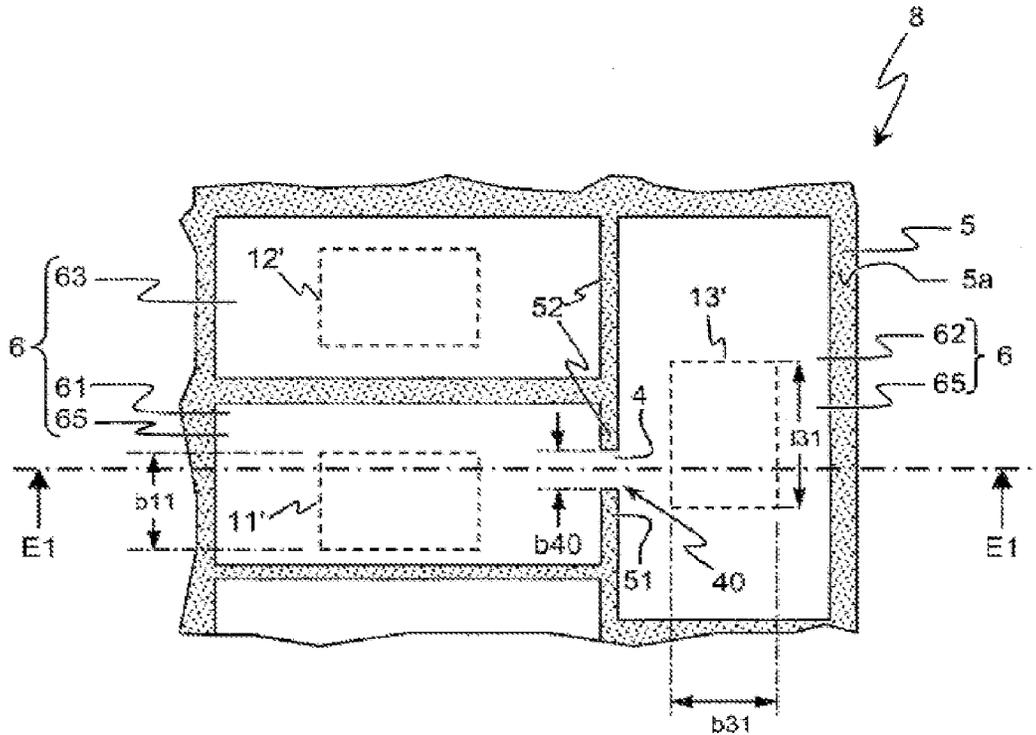
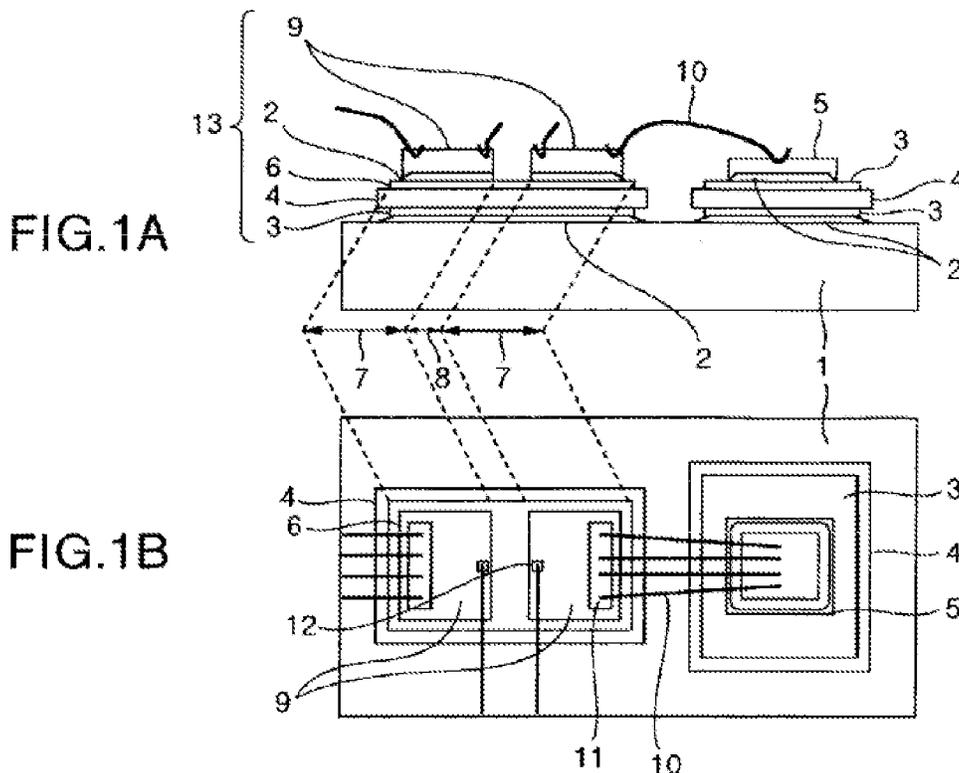


FIG 2A

Figure 2A shows an embodiment of a circuit carrier with a patterned metallization layer. Spec. ¶ 11. As shown in Figure 2A, a patterned metallization layer (6) is comprised of three sections (61, 62, and 63). Spec.

¶ 37. Sections 61 and 63 of the metallization layer are electrically conductively connected by connection 4. Spec. ¶ 37. In a disclosed embodiment, a semiconductor chip is mounted (and electrically conductively connected) to section 61, as indicated by area 11'. Spec. ¶ 39. Additionally, a shunt resistor is mounted (and electrically conductively connected) to section 62 (i.e., a second section of the metallization layer), as indicated by area 13'. Spec. ¶ 39.

The Examiner relies on, *inter alia*, Figures 1A, 1B, and 4 of Nakatsu (as well as corresponding portions of the Nakatsu's Specification) as teaching Appellants' claimed circuit arrangement. See Final Act. 3. Figures 1A and 1B of Nakatsu are illustrative and are reproduced below:



Figures 1A and 1B of Nakatsu are configuration views (a side view and a top view) showing an embodiment of Nakatsu's claimed power

converter comprising an electric current detector using a shunt resistor.
Nakatsu ¶¶ 1, 24.

Nakatsu states the shunt resistor is identified as item (13) and the semiconductor switching device as item (5). Nakatsu ¶ 41. As shown, semiconductor switching device (5) is mounted to metal foil layer (3) by solder (2) (i.e., providing an electrically conductive connection). Nakatsu teaches the shunt resistor (13) is constituted by three parts—the shunt resistance (8) and two main electrodes (7). Nakatsu ¶ 20. Nakatsu teaches “the shunt resistance 8 and the main electrodes 7 are formed out of one and the same sheet-like resistive plate 6.” Nakatsu ¶ 6. Additionally, Nakatsu states “[o]ne side of the shunt resistor 13 is fixedly attached to the *insulating layer* 4.” Nakatsu ¶ 20 (emphasis added). Opposite to the side of the shunt resistor attached to insulating layer (4), plates (9) are fixedly attached to the electrodes of the shunt resistor. Nakatsu ¶ 20.

Figure 1A of Nakatsu suggests that the shunt resistor assembly is mounted on a portion of metal foil layer (3) and, similarly, that semiconductor switching device/assembly is mounted to another portion of metal foil layer (3). However, as described in Nakatsu, electrical connectivity between the semiconductor switching device (5) and shunt resistor (13) is accomplished via aluminum wires (10). Nakatsu ¶ 41 (“constituting a main circuit of the inverter”). In other words, the electrically conductive connection between the two portions of the circuit arrangement in Nakatsu is not accomplished by electrically connecting the portions of the metal foil layer (i.e., the claimed metallization layer), but rather via aluminum wires (10).

For the reasons discussed *supra*, I do not find Nakatsu teaches, *inter alia*, “an electrically conductive connection between the first section [(of the metallization layer to which a semiconductor chip is electrically conductively connected)] and the second section [(to which the shunt resistor is electrically conductively connected)].”

Accordingly, I concur in the result reached by the Majority.