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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte VIVEK SUBRAMANIAN and VIKRAM PAVATE[1]

Appeal 2015-000093
Application 11/544,366
Technology Center 2600

Before DANIEL N. FISHMAN, JOHN F. HORVATH, and NABEEL U. KHAN, *Administrative Patent Judges*.

FISHMAN, *Administrative Patent Judge*.

DECISION ON REMAND

This application is on appeal before the Board on remand from the U.S. Court of Appeals for the Federal Circuit. *In re Subramanian*, Appeal 2017-1753 (Fed. Cir. December 26, 2017) (hereinafter "Order").

BACKGROUND

In a Final Office Action mailed May 15, 2013 ("Final Act."), the Examiner rejected all pending claims (1–6 and 8–42)[2] as follows.

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[1] Appellants identify Thin Film Electronics ASA as the real party in interest. App. Br. 1.

[2] Claim 7 was previously cancelled. App. Br. 37.

Claims 1–6, 8, 9, 15, 19, 20, and 23–38 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Bowers (US 5,883,582; Mar. 16, 1999), Yamazaki (US 2005/0146006 A1; July 7, 2005), and Carney (US 5,446,447; Aug. 29, 1995). Final Act. 2–14.

Claims 10–12 and 14 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Bowers, Yamazaki, Carney, and Jei (US 2005/0075079 A1; Apr. 7, 2005). Final Act. 14–16.

Claim 13 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Bowers, Yamazaki, Carney, and Van Eeden (US 6,154,136; Nov. 28, 2000). Final Act. 16–17.

Claim 16 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Bowers, Yamazaki, Carney, and Hashimoto (US 2005/0161783 A1; July 28, 2005). Final Act. 17–18.

Claims 17, 18, and 39–42 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Bowers, Yamazaki, Carney, and Kato (US 2005/0133790 A1; June 23, 2005). Final Act. 18.

Claims 21 and 22 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Bowers, Yamazaki, Carney, and Vega (US 6,362,738 B1; Mar. 26, 2002). Final Act. 18–19.

Appellants appealed to the Board under 35 U.S.C. § 134(a) from the Final Rejection. We entered a Decision on Appeal (mailed January 10, 2017) ("Decision" or "Dec.") affirming the Examiner's decision rejecting all pending claims. *Ex parte Subramanian*, Appeal 2015-000093. Appellants appealed to the Federal Circuit pursuant to 35 U.S.C. §§ 141 and 142 requesting reversal of our Decision. The Federal Circuit vacated our Decision and remanded the case for further consideration by the Board

consistent with the Federal Circuit's guidance that we "(1) consider a declaration submitted by Vivek Subramanian in the underlying proceedings and (2) enter a new final written decision." Order 1.[3]

On remand, we affirm the Examiner's decision rejecting all pending claims (1–6 and 8–42).

THE INVENTION

Appellants' invention is generally directed to structures and methods of manufacture for wireless identification tags, such as radio frequency ID ("RFID") tags. Spec. ¶ 2. RFID tag systems allow multiple tags to be read for identification information simultaneously. *Id.* ¶ 3. Reading RFID tags at a toll-road toll station is a typical application for simultaneously reading multiple RFID tags. *Id.* ¶ 5. Each vehicle passing through has an RFID tag with unique identification information. *Id.*

In such multi-tag applications, some technique must be employed to avoid collisions—i.e., multiple tags responding to a reader with information simultaneously. *Id.* ¶ 6. One simple approach for such collision avoidance is called "tags-talk-first" (or "TTF"). *Id.* In a TTF embodiment, each tag intermittently broadcasts its information when in the presence of an appropriate electric field. *Id.* In such TTF embodiments, it is desirable that each tag have a different time interval for its repeated broadcast in order to reduce the potential for collision between the identifying transmissions or retransmissions of multiple tags. *Id.* ¶ 7. However, conventional photolithography and deposition integrated circuit fabrication techniques

[3] Declaration Under 37 C.F.R. 1.132, submitted October 13, 2011 by co-inventor Vivek Subramanian ("Subramanian Declaration" or "Declaration").

make it difficult to create such variability among the response times of mass produced RFID IC tags—to the contrary, these techniques attempt to ensure uniformity among all fabricated circuits. *Id.* According to the application, prior known techniques designed a costly pseudo-random number generator within the tag circuit to generate randomized response time intervals for each tags' broadcast of information. *Id.* ¶ 8. However, such a circuit is complex and adds significant cost to the RFID tag circuits. *Id.*

Appellants claim to have solved these problems. In one exemplary embodiment, Appellants' tag includes a memory with an identifier and the memory includes a "printed layer." *Id.* ¶ 10. The "printed layer" is an integrated circuit layer fabricated by a printing technology including, for example, "laser printing, screen-printing, flexographic printing, offset printing, ink jetting, gravure printing, laser writing, and/or laser definition technology, perhaps using a metal nanoparticle- and/or liquid silane-based ink." *Id.* ¶ 11. That is, the "printed layer" is fabricated using circuit printing techniques rather than standard integrated circuit deposition and photolithography fabrication techniques. *Id.* As discussed above, in a TTF multi-tag application, the tag includes a silent period after transmitting and before re-transmitting its ID—the transmission time plus the silent period after each transmission define the tag's broadcast interval. *Id.* ¶ 12. The silent period for Appellants' tags is "dependent on various environmental and physical variables" of the printed layer thereby achieving randomization of the broadcast intervals among RFID tags without the need for costly, complex pseudo-random number generators. *Id.*; *see also id.* ¶¶ 30, 66.

Independent claim 1, reproduced below, is illustrative of Appellants' invention, with disputed limitations in italics:

> 1. A tag configured to wirelessly communicate with a reader in a multi-tag read capable system using a tags-talk-first (TTF) anti-collision scheme, the tag comprising:
>
> a) a memory portion storing a plurality of memory bits, the plurality of memory bits encoding an identifier for the tag, *said memory portion comprising at least one printed layer*; and
>
> b) a circuit configured to (i) transmit a bit string to the reader, said bit string being related to said identifier, (ii) cause said tag to remain silent for a unique silent period following complete transmission of said bit string, *said unique silent period being preset by said identifier or determined by variations in environmental parameters, physical parameters, and/or electrical performance of components within said tag, including in said printed layer(s) of the memory portion*, and (iii) retransmit said bit string after said unique silent period elapses, wherein said circuit comprises:
>
> (i) a power-up circuit coupled to an antenna, said antenna being configured to receive a radio frequency (RF) signal from said reader, and said power-up circuit being configured to provide an enable signal when said RF signal is received; and
>
> (ii) control and readout logic, comprising a plurality of thin film transistors (TFTs).

ANALYSIS

Only those arguments actually made by Appellants have been considered in this Decision. Arguments that Appellants did not make in the Briefs are waived. *See* 37 C.F.R. § 41.37(c)(1)(iv).

We have reviewed the Examiner's rejections in light of Appellants' arguments that the Examiner erred. App. Br. 7–34; Reply Br. 2–10. We have also reviewed the Subramanian Declaration. We are not persuaded by Appellants' contentions of Examiner error, including any error Appellants' attempt to prove by relying on Dr. Subramanian's Declaration. Accordingly,

we adopt as our own the Examiner's findings and reasons set forth in the Final Action and Answer. We highlight and address specific arguments and findings for emphasis as follows.

A. Rejection over Bowers, Yamazaki, and Carney

The Examiner rejected each of the independent claims (1, 15, 20, and 23) over the combined teachings of Bowers, Yamazaki, and Carney. Final Act. 2–5, 8–12.

A patent claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are "such that the subject matter[,] as a whole[,] would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains." *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations, including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) objective evidence of nonobviousness, i.e., "secondary considerations." *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

In weighing secondary considerations, "[o]bjective evidence of nonobviousness can include copying, long felt but unsolved need, failure of others, commercial success, unexpected results created by the claimed invention, unexpected properties of the claimed invention, licenses showing industry respect for the invention, and skepticism of skilled artisans before the invention." *Power Integrations, Inc. v. Fairchild Semiconductor Int'l, Inc.*, 711 F.3d 1348, 1368 (Fed. Cir. 2013) (citing *In re Rouffet*, 149 F.3d

1350, 1355 (Fed. Cir. 1998)). "These objective considerations can protect against the prejudice of hindsight bias, which often overlooks that '[t]he genius of invention is often a combination of known elements which in hindsight seems preordained.'" *Id.* (quoting *McGinley v. Franklin Sports, Inc.*, 262 F.3d 1339, 1351 (Fed. Cir. 2001)). "[E]vidence of secondary considerations may often be the most probative and cogent evidence in the record." *Stratoflex, Inc. v. Aeroquip Corp.*, 713 F.2d 1530, 1538 (Fed. Cir. 1983).

1. Level Of Ordinary Skill In The Art

Appellants do not present any argument regarding the level of ordinary skill in the art. We note, co-inventor Dr. Subramanian has a very high level of skill in the art as a professor of electrical engineering at the University of California, Berkeley possessing a Bachelor's degree, a Master's degree, and a Ph.D, all in electrical engineering. Declaration ¶¶ 1–2. Lacking any evidence in the record regarding the level of ordinary skill, we determine that the applied prior art reflects the appropriate level of skill at the time of the claimed invention. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001).

2. Scope And Content Of The Prior Art

a. Bowers

Bowers discloses methods and structures for reading multiple RFID tags. Bowers Abstract. Tags periodically transmit information followed by larger non-transmission intervals between each transmission. *Id.* The non-transmission interval of each tag is fixed, but randomly varies between tags

due to manufacturing tolerances in the electrical components that make up the tags. *Id.*; *id.* at 4:7–12. The variability of the non-transmission intervals among tags, due to manufacturing tolerances, causes tag transmissions to be less likely to overlap, thus, increasing the probability of a tag reader successfully receiving transmitted information from each of multiple tags. *Id.* at 4:12–25.

Bowers' tag includes programmable memory 18 storing information to be transmitted when power is applied to the tag. *Id.* at 5:11–16. The information stored in memory 18 may be any useful information including, for example, person or object identification, product identification and warranty information, location of manufacture of an object, etc. *Id.* at 5:16–34.

Bowers' tag also includes timer circuit 19 to count a predetermined amount of time after the tag transmits its stored information, during which the tag is not transmitting (i.e., the duration of the non-transmission interval). *Id.* at 5:35–40. The timing circuit is constructed using electrical components with a relatively wide degree of manufacturing tolerance (e.g., +/- 20%) such that the non-transmission interval between tags will vary due to the variability of the manufacturing tolerances of the components that make up the timing circuit. *Id.* at 8:17–26. Bowers further discloses,

> Thus, in operation, each device **10** within the interrogation zone theoretically transmits its memory data **36** at the same time, [however], in reality, variations in the electrical components comprising the timing circuit **19** cause the devices to transmit their memory data **36** at least slightly different times. In addition, even should two or more devices **10** initially transmit their memory data **36** at the same time or at overlapping times, because the length of the non-transmission interval **38** is much greater than the length of the transmission interval **36**, the non-

> transmission interval **38** among the devices should vary enough such that the next or a subsequent transmission interval **36** for each device **10** will likely occur at a different instant in time. Making the non-transmission interval **38** much greater than the transmission interval **36** and varying the tolerance of the fixed non-transmission interval **38** among the devices **10** has been found sufficient to ensure that when the number of devices **10** within the interrogation zone of the interrogator **20** is smaller than a predetermined interrogation duration divided by the duration of a single message transmission, all or a very high proportion of all of the devices **10** within the interrogation zone will be detected and the data transmitted therefrom read.

Id. at 8:37–59.

b. Yamazaki

Yamazaki relates to a thin film integrated circuit ("IC") such as may be used for securities. Yamazaki ¶ 1. According to Yamazaki, there was a need for an IC card or IC tag that provided wireless communications for automatic identification of associated objects such as securities and goods. *Id.* ¶ 2. Such IC tags needed to be small and inexpensive and usable on, for example, paper goods (securities). *Id.* Yamazaki discloses an ID chip (e.g., an IC tag) made from a thin film capable of mounting on securities, bills, belongings, food and drink containers, etc. (i.e., on paper and plastic goods). *Id.* ¶ 9. Yamazaki also discloses that the ID chip utilizes thin film transistors ("TFTs"). *Id.* ¶ 175.

In particular, Yamazaki discloses an exemplary ID chip that comprises a read-only memory ("ROM") for storing, for example, identification information. *Id.* ¶ 225. Specifically, Yamazaki discloses an ID chip with two ROMs (first ROM 110a and second ROM 110b). *Id.* Yamazaki further discloses the first ROM may be formed using standard

photolithography manufacturing techniques and the second ROM may be formed using ink jet printing manufacturing techniques. *Id.* ¶ 234. Ink jet printing manufacturing of the second ROM is useful for storing different circuit connections in each ID chip. *See id.* ¶ 244. Yamazaki discloses that the ROM (e.g., the second ROM formed using ink jet printing), may store data specific to that ID chip (i.e., a unique ID) "based on variations in characteristics of the semiconductor film." *Id.* ¶ 19. Yamazaki refers to these variations as a "fingerprint" that is relied on to produce random data in each ID chip. *See id.* ¶ 261. Specifically, Yamazaki discloses,

> Described in this embodiment mode are a circuit configuration and a manufacturing method of an ID chip using fingerprint. The use of the fingerprint can realize a memory that stores random fixed data by utilizing variations in characteristics of TFTs. Note that variations in characteristics of TFTs include variations due to grain patterns of a crystalline semiconductor film forming an active layer of a TFT and process variations (film thickness, film quality, impurity concentration and the like). A non-volatile memory that has the same circuit configuration and layout and stores random fixed data whenever it is manufactured even by using the same step is referred to as a random number ROM.

Id.

c. Carney

Carney discloses a radio frequency ("RF") tagging system supporting a large number of tag identification codes without increasing the size of the tags. Carney Abstract. In particular, the tags of Carney each include receiver 368 that, in turn, includes an RF-to-DC converter for converting a received radio frequency signal (i.e., from a tag reader station) into electrical energy for powering various circuits of the tag). *Id.* at 12:4–15.

3. Differences Between The Prior Art And The Claimed Subject Matter Of Independent Claims 1, 15, 20, And 23

a. Examiner's Findings

In rejecting independent claim 1, the Examiner finds Bowers discloses a tag for wireless communications with a reader. Final Act. 2 (citing Bowers 2:30–47). The Examiner further finds Bowers discloses the tag comprises a memory having an identifier. *Id.* (citing Bowers 4:26–32, 5:11–13, Fig. 1 (tag or device 10)). Still further, the Examiner finds Bowers discloses the recited "circuit configured to provide a bit string followed by a unique silent period . . . ." *Id.* at 3 ("a *non-transmission interval* (considered a 'silent period') that is considered 'unique' because it *varies between tags due to manufacturing tolerances in the construction of electrical components within each tag*. One of ordinary skill in the art would have recognized that the manufacturing tolerances in the construction of the electrical components would affect the 'electrical performance of components' within the tag, thus causing a uniqueness of the 'silent period.'" (citing Bowers 4:1–15)). The Examiner also finds "Bowers must include 'control and readout logic' [as claimed] in order to output the bit stream." *Id.* (citing Bowers 5:14–19).

The Examiner finds a difference between Bowers and claim 1 in that Bowers does not expressly disclose that the control and readout logic comprises a plurality of thin film transistors or that the memory comprises at least one printed layer. *Id.* However, the Examiner finds Yamazaki in the proposed combination discloses an ID chip having a memory formed using an ink jet printing process and discloses that the ID chip uses a plurality of thin film transistors. *Id.* (citing Yamazaki ¶¶ 154, 167, 225, 230, 233, 234, 244).

The Examiner reasons the ordinarily skilled artisan would have been motivated to combine Bowers and Yamazaki to "obtain memory cells with improved frequency characteristics and operating margin . . . and to achieve cost reduction of the ID chip." *Id.* at 4 (citing Yamazaki ¶¶ 154, 235).

The Examiner also finds Bowers discloses the recited antenna but does not expressly disclose the recited power-up circuit coupled with the antenna. *Id.* (citing Bowers 2:30–40, 2:58–3:3, 4:39–45). However, the Examiner finds Carney in the proposed combination discloses the recited power-up circuit as receiver means 368 in a radio frequency tag—receiver means 368 including an RF-to-DC converter and energy storage (e.g., a capacitor), coupled to antennas (288, 306, 324), to convert received radio frequency signals into electrical energy for operating various components of the tag. *Id.* (citing Carney 12:4–15, Fig. 18 (receiver 368)).

The Examiner reasons the ordinarily skilled artisan would have been motivated to combine Bowers, Yamazaki, and Carney "to provide the data at the resonant frequency disclosed by Bowers, using known and commercially acceptable technology and techniques to render the system commercially advantageous." *Id.* at 4–5 (citing Carney 3:4–8).

Accordingly, the Examiner has established a prima facie case of obviousness of independent claim 1 by identifying the legal basis for the rejection (obviousness under 35 U.S.C. § 103), identifying each element of the claim in the combined teachings of Bowers, Yamazaki, and Carney, and articulating reasons the ordinarily skilled artisan would have been motivated to combine the references. *See In re Jung*, 637 F.3d 1356, 1363 (Fed. Cir. 2011). The Examiner applies similar combined disclosures of Bowers, Yamazaki, and Carney in rejecting similar limitations of independent claims

15 (Final Act. 8–10), 20 (*id.* at 11), and 23 (*id.* at 12). Having established a prima facie case of obviousness, the burden shifts to Appellants to persuasively rebut the Examiner's case. *See Jung*, 637 F.3d at 1365.

b. Appellants' Arguments

Appellants argue the rejection of claims 1–6, 8, 9, 15, 19, 20, and 23–38 together. App. Br. 2–20. Initially, we observe that essentially every argument presented by Appellants cites a corresponding paragraph of the Subramanian Declaration. Each corresponding paragraph of the Declaration is nearly identical to the argument in Appellants' Appeal Brief. For example, Appellants argue,

> Furthermore, the cited references neither disclose nor suggest the advantages of such a tag, method and system, including simplifying the approach for multi-tag EAS, HF, UHF and RFID systems using TTF anti-collision schemes without incorporating relatively complex circuits such as pseudo-random number generators (see paragraph 55 of the Declaration of Subramanian submitted October 14, 2011).
>
> Additionally, the cited references neither disclose nor suggest potential issues associated with integrated circuitry including printed layers (e.g., film morphology, topography, adhesion and/or subsequent processing), nor do they suggest solutions thereto (see paragraph 56 of the Declaration of Subramanian). As a result, one of ordinary skill in the art would not recognize from reading the cited references the advantages of, or the technical challenges faced by, the invention defined in the present Claims 1, 15, 20 and 23 (see, e.g., paragraph 57 of the Declaration of Subramanian).

App. Br. 9. The cited paragraphs 55–57 of the Subramanian Declaration read as follows:

> 55. Furthermore, the cited references neither disclose nor suggest the advantages of such a tag, method and system, including simplifying the approach for multi-tag EAS, HF, UHF and RFID systems using TTF anti-collision schemes without incorporating relatively complex circuits such as pseudo-random number generators.
>
> 56. Additionally, the cited references neither disclose nor suggest potential issues associated with integrated circuitry including printed layers (e.g., morphology, topography, adhesion and/or subsequent processing), nor do they suggest solutions thereto.
>
> 57. As a result, one of ordinary skill in the art would not necessarily recognize from reading the cited references the advantages of or the technical challenges faced by the invention defined in paragraphs 6-9 above.

Comparing the above portion of the Appeal Brief with the cited paragraphs of the Subramanian Declaration reveals identity of the arguments with only a minor syntactic change to refer to the independent claims (1, 15, 20, and 23) as opposed to the related paragraphs of the Declaration (paragraphs 6–9 that merely recite the language of independent claims 1, 15, 20, and 23, respectively). The Appeal Brief is replete with such citations to the Subramanian Declaration such that most arguments in the Appeal Brief that cite to the Subramanian Declaration are identical to, or substantively identical to, the cited portion of the Declaration. Although we acknowledge Dr. Subramanian's significant expertise, we also weigh the inherent bias and potentially self-serving nature of the declaration of a co-inventor as distinct from that of an independent expert.

Considering the Appellants' briefs and Declaration together, we analyze the arguments presented in Appellants' Brief and the corresponding, nearly identical, portions of the Subramanian Declaration as follows.

i. Not All Elements Are Taught Or Suggested

Appellants broadly assert "[n]o possible combination of Bowers et al., Yamazaki et al. and Carney et al. discloses or suggests a tag" as recited in the independent claims. App. Br. 8–9. We are not persuaded by Appellants' arguments that the Examiner erred.[4] Initially, we agree with the Examiner that Appellants' arguments improperly attack the references individually rather than addressing the teachings or suggestions of the proposed combination. Ans. 7; *see In re Keller*, 642 F.2d 413, 425 (CCPA 1981).

Appellants admit that, in Bowers, "[t]he non-transmission intervals are fixed for a given tag, but are random between tags due to manufacturing tolerances in electrical components from which the tag is constructed." App. Br. 16; *see also* Subramanian Declaration ¶ 30. Appellants further admit "Bowers et al. discloses utilizing the variability in manufacturing tolerances of electrical components between tags" but Appellants argue "Bowers et al. is silent with regard to how the tags are manufactured." *Id.*; *see also* Declaration ¶ 31. Appellants contend,

> because Bowers does not teach or suggest a memory that has at least one printed layer, Bowers cannot reasonably be considered to teach or suggest a unique silent period that is preset by an identifier or determined by variations in environmental parameters, physical parameters, and/or electrical performance of components within a printed layer.

[4] Appellants and the Examiner disagree as to whether the phrase "printed layer" is deserving of patentable weight. *See* Ans. 4; *see also* Reply Br. 2–6. We do not reach this issue because, even granting "printed layer" patentable weight, the Examiner finds, and we agree, the proposed combination meets the limitations of claim 1. *See* Final Act. 2–5; *see also* Ans. 4–8.

Id. We note the Examiner relies on Yamazaki for teaching manufacturing an RFID tag memory (ROM) having at least one printed layer. Final Act. 3.

Appellants admit that Yamazaki "discloses that the ROMs can be formed by ink jet printing." App. Br. 17; *see also* Subramanian Declaration ¶ 32. Appellants further admit Yamazaki discloses memory circuits that store data in an ID chip and that the stored data may be randomized data based on variations in the characteristics of the thin film transistors formed on the chip. *Id.* at 17–18; *see also* Declaration ¶ 34. Additionally, Appellants admit that Yamazaki discloses that the variations in the randomized data (based on variations in the thin-film transistors) include variations based on the ink jet printing process ("film thickness, film quality, impurity concentration and the like"). *Id.* at 18 (citing Yamazaki ¶ 261 and Fig. 14); *see also* Declaration ¶ 35. Still further Appellants admit that using printing techniques inherently forms printed circuits or layers having more variable "electrical, chemical, structural and/or physical characteristics and/or properties," and that this inherent variance in the printed circuit layers "would be recognized by persons of ordinary skill." *Id.* at 12 (citing Declaration ¶ 16).[5] However, Appellants contend Yamazaki fails to disclose the benefit of using the inherent variations in its printed circuit layer to determine the unique silent period for a tag, specifically contending,

> although Yamazaki et al. discloses that the ROMs can be formed by ink jet printing, Yamazaki et al. does not teach or suggest a unique silent period that is preset by an identifier or determined by variations in environmental parameters, physical parameters, and/or electrical performance of components within a printed layer.

[5] See further analysis below regarding inherency issues.

Id. at 19. We note the Examiner relies on Bowers for teaching an RFID tag having a unique silent period determined by variations in the manufacturing tolerances of electrical components within the tag. Final Act. 3.

As noted above, the Examiner's proposed combination of Bowers, Yamazaki, and Carney relies on Bowers, not Yamazaki, for teaching variations in the silent period among tags based on variations within a wider range of manufacturing tolerances; and relies on Yamazaki, not Bowers, for teaching the use of an ink jet printing manufacturing technique, with its inherently greater variability when compared to standard integrated circuit fabrication techniques to produce the recited printed layer within the memory portion to generate a unique data in each tag to cause each tag to have a unique silent period. Specifically, the Examiner finds the combined teachings of Bowers and Yamazaki teach or suggest a tag that varies the non-transmission interval among tags as a function of manufacturing tolerances (as disclosed in Bowers) by using ink jet printing techniques (as disclosed in Yamazaki). Final Act. 3–4.

We agree with the Examiner's findings and adopt them as our own. Bowers expressly discloses randomized non-transmission intervals (i.e., "silent periods" as claimed) between tags, where the randomization of the intervals is achieved due to variations in manufacturing tolerances of components in the tags. *See* Bowers Abstract, 2:21–24, 4:7–15, 8:17–59, 9:20–27. Yamazaki discloses a memory having a "printed layer" (i.e., using ink jet printing), as relied upon by the Examiner, for generating circuits of an ID chip with randomized data based on variations in the thin-film transistors generated by an ink jet printing process. Yamazaki ¶ 261.

In like manner, Appellants argue "Carney et al. is silent with regard to how tags are manufactured" failing to use terms such as "deposit," "photo," "TFT," or "film" as they would relate to a manufacturing process for an RFID tag. App. Br. 19. Thus, Appellants contend "Carney et al. cannot disclose or suggest a tag" such as recited in the independent claims. *Id.* at 19–20; *see also* Declaration ¶ 38. Appellants further contend, "[i]n particular, Carney et al. does not teach or suggest a unique silent period that is preset by an identifier or determined by variations in environmental parameters, physical parameters, and/or electrical performance of components within a printed layer." *Id.* at 20.

Again, we agree with, and adopt as our own, the Examiner's findings regarding Carney. The Examiner relies on the combined teachings of Bowers and Yamazaki, not Carney, for disclosing an ink jet printing process for manufacture of RFID tags having unique silent periods as discussed *supra*. Carney is relied on in the proposed combination for disclosing the recited "power-up circuit." Final Act. 4.[6]

As noted *supra*, the Examiner finds, and we agree, that Appellants' arguments improperly attack the references individually rather than addressing what the combined disclosures teach or suggest. In response,

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[6] Although we do not rely on the following findings, we note that like Carney, both Bowers and Yamazaki disclose a power-up circuit coupled to an antenna as a standard component of RFID tags. *See Bower*, 6:3–15, Figs. 1, 2 (disclosing RFID device 10 includes IC 14 that "internally rectifies the induced AC voltage at the ANT input to provide an internal DC voltage source"); *see also* Yamazaki ¶¶ 225, 237, Fig. 11 (disclosing ID chip 522 includes "RF circuit **103** [that] receives an analog signal from the antenna **515** and outputs from the antenna **515** an analog signal received from the data modulation circuit **108**. The power source circuit **104** generates a constant power source from a received signal.").

Appellants assert "[a] reference discloses only what it contains." Reply Br. 9. Appellants then contend "[l]ogically, if none of the individual cited references disclose or suggest the claimed feature or its advantages, then no possible combination of the cited references can disclose or suggest the claimed features or its advantages." *Id.* We remind Appellants "a reference must be considered not only for what it expressly teaches, but also for what it fairly suggests." *In re Bell*, 991 F.2d 781, 785 (Fed. Cir. 1993) (quoting *In re Burckel*, 592 F.2d 1175, 1179 (CCPA 1979)). Furthermore,

> [t]he test for obviousness is not . . . that the claimed invention must be expressly suggested in any one or all of the references. Rather, *the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art.*

Keller, 642 F.2d at 425 (citations omitted; emphasis added). Thus, although none of Bowers, Yamazaki, or Carney, alone, discloses *all* features of the independent claims, we are not persuaded the Examiner erred in finding the *combination* of Bowers, Yamazaki, and Carney teaches or suggests all features of independent claims 1, 15, 20, and 23.

The Examiner also finds the same combination of Bowers, Yamazaki, and Carney teaches or suggests all features of claims 2–6, 8, 9, 19, and 24–38, which depend variously (directly or indirectly) from one of independent claims 1, 15, 20, and 23. *See* Final Act. 2–14. Appellants do not separately argue with particularity the rejection of claims 2–6, 8, 9, 19, and 24–38 (App. Br. 20). Thus, the Board may consider the patentability of these claims on the same basis as the patentability of the independent claims from which they depend. *See* 37 C.F.R. § 41.37(c)(1)(iv). Moreover, we are not persuaded the Examiner erred in finding the combined disclosures of Bowers, Yamazaki, and Carney teaches or suggests the features of

dependent claims 2–6, 8, 9, 19, and 24–38. Therefore, we agree with, and adopt as our own, the Examiner's findings (Final Act. 2–14) that the proposed combination of Bowers, Yamazaki, and Carney teaches or suggests all features of independent claims 1–6, 8, 9, 15, 19, 20, and 23–38.

ii. Reasons To Combine References

The Examiner finds the ordinarily skilled artisan would have combined Yamazaki with Bowers "to obtain memory cells with improved frequency characteristics and operating margin (Yamazaki et al., Para. [0235]), and to achieve cost reduction of the ID chip (Yamazaki, Para. [0154])." Final Act. 3–4. The Examiner further finds it would have been obvious to the ordinarily skilled artisan to combine Carney with Bowers and Yamazaki "by using a simplified version of Carney's invention (e.g., one antenna and resonant circuit of Fig. 18) to provide the data at the resonant frequency disclosed by Bowers, using known and commercially acceptable technology and techniques to render the system commercially advantageous (Carney, Col. 3, lines 4-8)." *Id.* at 4–5.

Appellants to not present any argument directly challenging the Examiner's articulated reasons to combine the references.

We agree with, and adopt as our own, the Examiner's reasoning that the ordinarily skilled artisan would have combined Bowers, Yamazaki, and Carney. A reason to combine teachings from the prior art "may be found in explicit or implicit teachings within the references themselves, from the ordinary knowledge of those skilled in the art, or from the nature of the problem to be solved." *WMS Gaming, Inc. v. Int'l Game Tech.*, 184 F.3d 1339, 1355 (Fed. Cir. 1999) (citing *Rouffet*, 149 F.3d at 1355). Here, the

Examiner has articulated a reason to combine the references based on rational underpinnings—i.e., all three references relate to RFID tag technology and the Examiner's articulated reasons to combine are based on express disclosures of improvements for RFID tags in both Yamazaki and Carney.

iii. Inherency

In an earlier response to an Office Action, Appellants apparently asserted "the phrase 'printed layer' recited in claims 1, 15, and 23 refers to a thin film having electrical, chemical, structural and/or physical characteristics and/or properties different from and more variable than a thin film defined by conventional photolithographic processing." Final Act. 21 (quoting from an earlier response by Appellants). In the Final Office Action, the Examiner responded to this remark suggesting the claims fail to recite any such properties as limitations of the claims. *Id.* Responsive to this observation by the Examiner, Appellants argue:

> In the present case, evidence has been submitted which makes clear that the electrical, chemical, structural and/or physical characteristics and/or properties of a "printed layer" are different from and more variable than a thin film defined by conventional photolithographic processing (see paragraph 16 of the Declaration of Subramanian), and that this would be recognized by persons of ordinary skill. Therefore, there is no need to recite in the claims the characteristics and/or properties of a printed layer, as such characteristics and/or properties are *inherent* in a printed layer.

App. Br. 12 (citing Declaration ¶ 16) (emphasis added). Comparing a printed layer with traditional circuit constructs (e.g., photolithographic and deposition techniques), Appellants contend printed layers have different "purity of the materials" and exhibit different "electrical properties and

characteristics" (*id.* (citing Declaration ¶ 17)), exhibit different "edge definition" (*id.* (citing Declaration ¶ 18)), have different resistivity (*id.* at 13 (citing Declaration ¶ 19)), "have dimensions that deviate from linearity" (*id.* (citing Declaration ¶ 20)). Thus, Appellants contend, "the structure and properties of printed layers are different from the structure and properties of photolithographically patterned thin film layers, even when the layers have substantially the same composition (e.g., are the same metal or include a mixture of the same metals in the same atomic ratio) and have similar dimensions" (*id.* (citing Declaration ¶ 21)). As noted above, however, Appellants' admit in their Appeal Brief that these noted differences between printed and photolithographically patterned thin film layers are "inherent in a printed layer," and would have been recognized by persons of ordinary skill in the art. *Id.* at 12.

We agree with the Examiner that the benefits and issues associated with variations in environmental and physical parameters of circuits manufactured using printing techniques are inherent in the use of such printing techniques and, thus, similarly inherent in the ink jet printing techniques disclosed by Yamazaki for ID tag circuit generation. *See* Ans. 6. Appellants' claims do not require specific steps in the manufacture of, or structure of, the printed layer to realize the benefits of variations in the silent period of a tag derived from use of printing techniques. Instead, Appellants' claims merely rely on the *inherent* benefits (and drawbacks) in the use of printing techniques to achieve variations in the silent period between tags. It is precisely those same *inherent* benefits (and drawbacks) that the Examiner relies on in the combination of Bowers and Yamazaki to teach generating desired randomization in the silent period between tags (as taught in

Bowers) based on manufacturing variability of ink jet printing to randomize data in a circuit (as taught in Yamazaki).

Although admitting that these variabilities are inherent in the recited printing techniques, Appellants contend the applied prior art references fail to "suggest that such inherent characteristics and/or properties are useful and/or beneficial in a tag configured to communicate in a tags-talk-first (TTF) wireless communication system." Reply Br. 6–7. We remain unpersuaded. "[I]t is elementary that the mere recitation of a newly discovered function or property, inherently possessed by things in the prior art, does not cause a claim drawn to those things to distinguish over the prior art." *In re Swinehart*, 439 F.2d 210, 212–13 (CCPA 1971). Moreover, regardless of whether these benefits are inherent in a printed layer, as discussed *supra*, we agree with the Examiner that the combined teachings of Bowers, Yamazaki, and Carney teach or suggest the claimed features.

Appellants' invention is not directed to a particular new process that exhibits these differences from traditional circuit manufacturing techniques but is, instead, directed to a known printing process for manufacture of circuit—a printing process with these inherent differences from traditional circuit fabrication techniques. Yamazaki clearly discloses a known ink jet printing process, and relies on the inherent variability of that process to generate unique IDs in a ROM memory of a tag circuit. Appellants admit this. *See* App. Br. 18 (citing Yamazaki ¶ 261 and Fig. 14 ("The use of the fingerprint can realize a memory that stores ***random fixed data*** (e.g., an identification number) by utilizing variations in the characteristics of TFTs.")); *see also* Declaration ¶¶ 34, 35.

Accordingly, we determine the variations in electrical circuits manufactured as a "printed layer" as compared to traditional circuit manufacturing techniques (such as deposition and photolithography) are inherent aspects of a known process, and Appellants have admitted such in its arguments. App. Br. 12–13; Reply Br. 6–7.

4. Secondary Considerations

As noted *supra*, secondary considerations may include "unexpected properties of the claimed invention" and "skepticism of skilled artisans before the invention." *Power Integrations*, 711 F.3d at 1368. Appellants may show that the claimed invention has an unexpected property over the prior art "with evidence that the claimed invention exhibits some superior property or advantage that a person of ordinary skill in the relevant art would find surprising or unexpected." *In re Mayne*, 104 F.3d 1339, 1343 (Fed. Cir. 1997). An examination for unexpected results is a factual, evidentiary inquiry. *Id.*

Appellants do not present any arguments expressly framed in terms of "secondary considerations" or "objective indicia." However, some of Appellants' arguments suggest that using a printing process to produce a "printed layer" to determine a non-transmission interval for each tag produces the unexpected result that each tag's non-transmission interval is unique due to variability in the printed layer. For example, Appellants argue the cited references "neither disclose nor suggest the advantages of . . . a tag" generated using a printing process to form a printed layer and "neither disclose nor suggest potential issues associated with integrated circuitry including printed layers . . . nor do they suggest solutions thereto." App. Br.

9 (citing Declaration ¶¶ 55–57). Appellants further argue, "prior to the present invention, there was some uncertainty as to whether the processability of printed layers would render a device containing a printed layer unreliable and/or non-manufacturable." *Id.* at 13 (citing Declaration ¶ 22). Specifically, Appellants assert insulator layers are sometimes thickened to reduce breakdown problems but such techniques present problems for a printed insulator layer. *Id.* (citing Declaration ¶ 23).

We remain unpersuaded of Examiner error. The combined teachings of the prior art references relied upon directly contradict Appellants' assertion that the prior art fails to disclose the advantages of using a printed layer to generate variability in non-transmission intervals, or that such advantages would have been unexpected. As discussed *supra*, Bowers clearly discloses it was known to rely on a wider range of manufacturing tolerances to generate tag circuits with varying non-transmission intervals. Bowers Abstract, 4:7–12, 8:19–28, 9:11–27. Although Bowers does not disclose a specific fabrication technique to achieve such variances in manufacturing tolerances, Yamazaki clearly discloses it was known that ink jet printing processes could be used for that purpose. Specifically, Yamazaki discloses manufacturing the thin-film transistors of a ROM memory using an ink jet printing process *because* that process generates varying identifiers in the ROM memory of an ID chip. Yamazaki ¶ 261. Furthermore, Appellants have admitted to such disclosures of Bowers and Yamazaki. *See, e.g.*, App. Br. 16–18. Thus, contrary to Appellants' and Dr. Subramanian's assertions that the claimed use of a "printed layer" to generate non-transmission intervals produces the unexpected result that the non-transmission intervals are uniquely variable, the combined teachings of

the prior art references of Bowers and Yamazaki provide substantial evidence that it was expected that variability in manufacturing tolerances, such as the variable tolerances generated by using an ink jet printing process, could be used to generate an RFID tag circuit with varying data among multiple tags (including varying non-transmission intervals among the multiple tags).

The prior art also contradicts Appellants' assertion that "prior to the present invention, there was some uncertainty as to whether the processability of printed layers would render a device containing a printed layer unreliable and/or non-manufacturable." *Id.* at 13 (citing Declaration ¶ 22). Yamazaki clearly discloses the usability (processability and manufacturability) of ink jet printing processes to generate randomized data in a ROM of a tag. Yamazaki recognized not only the benefit of using a "printed layer" to introduce needed variability into the manufacturing process, but also the benefit of reduced manufacturing costs in its invention for generating randomized identifiers in the ROM of a tag. *See, e.g.*, Yamazaki Abstract, ¶¶ 8, 12, 30, 62, 65, 69, 71, 111, 138, 154, 256, 274.

5. Conclusion Regarding Obviousness Over Bowers, Yamazaki, and Carney

For the reasons expressed above, we are not persuaded the Examiner erred in rejecting independent claim 1. Independent claims 15, 20, and 23 include similar disputed limitations and are argued together with claim 1. *See* App. Br. 8–20. Thus, for the same reasons as claim 1, we are not persuaded the Examiner erred in rejecting independent claims 15, 20, and 23. Furthermore, Appellants do not separately argue with particularity the rejection of dependent claims 2–6, 8, 9, 19, and 24–38, dependent variously

from independent claims 1, 15, 20, and 23. *Id.* at 20. Thus, we sustain the rejection of claims 1–6, 8, 9, 15, 19, 20, and 23–38.

B. Other Rejections

All other rejections are based on the combination of Bowers, Yamazaki, and Carney, as discussed *supra*, in view of one or more other references—namely: Jei, Van Eeden, Hashimoto, Kato, and Vega. Regarding the remaining rejections, Appellants argue the additional references (Jei, Van Eeden, Hashimoto, Kato, and Vega) fail to cure the alleged deficiencies of Bowers, Yamazaki, and Carney. App. Br. 20–34. As discussed *supra*, we are not persuaded of the alleged deficiencies in the Examiner's application of Bowers, Yamazaki, and Carney. Thus, for the same reasons as claim 1, we sustain the rejection of claims 10–14, 16–18, 21, 22, and 39–42.

DECISION

We affirm the Examiner's decision to reject claims 1–6 and 8–42.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED