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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte ZVI OR-BACH, BRIAN CRONQUIST, ISRAEL BEINGLASS,
J. L. DE JONG, DEEPAK C. SEKAR, and PAUL LIM

Appeal 2014-005030¹
Application 12/970,602²
Technology Center 2800

Before MAHSHID D. SAADAT, CHARLES J. BOUDREAU, and
ADAM J. PYONIN, *Administrative Patent Judges*.

BOUDREAU, *Administrative Patent Judge*.

DECISION ON APPEAL

Appellants appeal under 35 U.S.C. § 134(a) from the Final Rejection of claims 13–17, 20, 21, 25, and 39–54.³ We have jurisdiction under 35 U.S.C. § 6(b).

We affirm-in-part and enter new grounds of rejection under 35 U.S.C. § 103, pursuant to our authority under 37 C.F.R. § 41.50(b).

¹ The record includes a transcript of the oral hearing held August 8, 2016.

² According to Appellants, the real party in interest is MonolithIC 3D Inc. Appeal Br. 3.

³ Claims 1–12, 18, 19, 22, 23, and 26–38 have been cancelled, and claim 24 has been allowed. Appeal Br. 5; Final Act. 14.

STATEMENT OF THE CASE

Introduction

Appellants' disclosure relates to integrated circuit devices and fabrication methods. Spec. ¶ 2. Of the rejected claims on appeal, claims 13, 46, and 51 are independent. Claim 13 is reproduced below for reference:

13. A method of manufacturing a semiconductor wafer, the method comprising:

providing a base wafer comprising a semiconductor substrate and a metal layer, said metal layer comprising aluminum or copper, and then

transferring a first mono-crystalline layer on top of said metal layer,

wherein said metal layer is in-between said base wafer and said first mono-crystalline layer, and said transferring said first mono-crystalline layer comprises an ion-cut, and

subsequently to said transferring,

processing said first mono-crystalline layer to define first transistors,

wherein said processing comprises at least two etch steps respectively defining an isolation for said first transistors and defining gates of said first transistors.

References and Rejections

Claims 13, 14, 39, 46, 48, and 51 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Lee (US 2004/0262635 A1, published Dec. 30, 2004). Final Act. 3.

Claims 15 and 25 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Lee and Temmler (US 2008/0194068 A1, published Aug. 14, 2008). Final Act. 7.

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Claim 16 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Lee and Gill (US 5,162,879, issued Nov. 10, 1992). Final Act. 8.

Claims 17, 47, and 52 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Lee and Gonzalez (US 2003/0059999 A1, published Mar. 27, 2003). Final Act. 9.

Claim 20 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Lee and Yu (US 2008/0124845 A1, published May 29, 2008) (hereinafter “Yu”). Final Act. 9.

Claim 21 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Lee and Mukasa (US 2008/0283875 A1, published Nov. 20, 2008). Final Act. 10.

Claim 40 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Lee and Rayssac (US 2004/0175902 A1, published Sept. 9, 2004). Final Act. 11.

Claims 41, 44, 49, and 53 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Lee and Yamazaki (US 2002/0096681 A1, published July 25, 2002). Final Act. 12.

Claims 42 and 43 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Lee and Kamiyama (US 2006/0118935 A1, published June 8, 2006). Final Act. 12.

Claims 45, 50, and 54 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Lee and Ahn (US 2008/0248618 A1, published Oct. 9, 2008). Final Act. 13.

ANALYSIS

We have reviewed the Examiner’s rejections in light of Appellants’ arguments that the Examiner erred. Except as indicated below with respect to claims 14, 16, 39, 48, and 51–54, we disagree with Appellants that the Examiner erred and adopt as our own the findings and conclusions set forth by the Examiner in the Final Action from which this appeal is taken and the Examiner’s Answer. We highlight and address specific findings and arguments for emphasis as follows.

Claims 13 and 46

The Examiner finds Lee discloses all elements of independent claims 13 and 46. Final Act. 3–6. With respect specifically to the limitation “wherein . . . said transferring said first mono-crystalline layer comprises an ion-cut” recited in each of those claims, the Examiner finds Lee discloses “‘smart cut’ . . . which is a well known term in the art for implanting ions to a given layer, thus weakening the structure, and breaking or ‘cutting’ along this weakened layer.” *Id.* at 4–6 (citing Lee ¶ 98). Appellants do not dispute that Lee discloses ion-cut (*see* Tr. 14:13–14 (stating that “SmartCut” is a tradename for “ion-cut”); *see also* Spec. ¶¶ 97, 99 (identifying SmartCut and stating in reference thereto that such “use of an implanted atomic species . . . to create a cleaving plane . . . may be referred to in this document as ‘ion-cut’ and is generally the illustrated layer transfer method”)), as well as all other elements of independent claims 13 and 46, but contend that “Lee does not disclose an *enabled* method wherein ‘. . . said transferring said first mono-crystalline layer comprises an ion-cut[,]’ as recited by claims 13, 46 and 51” (Appeal Br. 14 (italics added)). In particular, according to

Appellants, the high dosage of ions utilized in the SmartCut process used by Lee creates damage to the silicon lattice. Appellants further contend that one specific company, Soitec, utilizes 1100–1200 °C thermal anneals to repair such damage as part of the SmartCut process in the manufacture of silicon on insulator (SOI) wafers, but that “[t]hese damage repair anneals are not compatible with the commonly used, low melting point, interconnect metals (for example, copper and aluminum) of the lower device layer in a 3D stack.” *Id.* Appellants further contend that “the passage of the high dosage of ions utilized in the SmartCut process [also] creates a lower level of damage to the silicon lattice of the bulk of the to-be-transferred donor layer as the ions pass through it,” and “[a]nnealing of this type of lattice damage requires temperatures of about 600°C or greater, which again is incompatible with the commonly used, low melting point, interconnect metals.” *Id.* In alleged support of their contentions, Appellants cite certain continuations and continuations-in-part of Lee, an article, and an Internet video, in which, Appellants allege, “inventor Lee agrees with these issues with SmartCut in general with respect and as applied to his inventions.” *Id.* at 15–18; Reply Br. 3–9.

Appellants’ contentions are not persuasive. A patent cited as prior art is presumed to be enabled.⁴ *Amgen, Inc. v. Hoechst Marion Roussel, Inc.*, 314 F.3d 1313, 1354 (Fed. Cir. 2003). Moreover, “proof of efficacy is not required for a prior art reference to be enabling for purposes of anticipation.” *Impax Labs. v. Aventis Pharm. Inc.*, 468 F.3d 1366, 1383 (Fed. Cir. 2006)

⁴ Lee issued as U.S. Patent No. 7,052,941 B2 on May 30, 2006, containing in all relevant parts the same disclosure as the published application cited by the Examiner.

(citation omitted). Rather, when a prior art reference expressly anticipates all of the elements of a claimed invention, the reference is presumed to be operable and the burden is on the applicant to provide facts rebutting the presumption of operability. *In re Sasse*, 629 F.2d 675 (CCPA 1980).

Although direct evidence in the form of declarations or affidavits is not required for an applicant to rebut the presumption that a reference is enabling, “an applicant must generally do more than state an unsupported belief that a reference is not enabling.” *In re Morsa*, 713 F.3d 104, 110 (Fed. Cir. 2013).

We agree with the Examiner that Lee’s later publications cited by Appellants are not persuasive to show that Lee does not provide an enabling disclosure with respect to the claims on appeal. Ans. 16. As the Examiner explains, the test of enablement requires that experimentation by one of ordinary skill in the art must not be undue or unreasonable (MPEP 2164.01). Appellants’ argument that Lee’s disclosure of the use of the SmartCut process would be unsuitable for the claimed method is undermined by Appellants’ own Specification describing SmartCut as being “referred to . . . as ‘ion-cut’” and as being “generally the illustrated layer transfer method.” Spec. ¶ 99. The Examiner finds, and we agree, that Lee’s subsequent publications merely provide warnings that SmartCut may result in damage in some circumstances, not that SmartCut causes damage that “must always be removed by thermal anneals that always would damage the interconnect metals.” Ans. 16. Thus, although those publications suggest that some optimization might be called for, Appellants have provided no persuasive evidence that such optimization would rise to the level of undue or unreasonable experimentation for a person of ordinary skill in the art. *See*

id. at 16–17. Appellants contend in the Reply Brief, without supporting evidence,⁵ that “one of ordinary skill in the art knows that the Hydrogen dose required to induce a cleave *by its very nature* is at a level that will induce damage at/near the implanted depth”; that “[i]t is not a matter of ‘optimization’ and ‘experimentation’”; and that “[i]on-cut damage cannot be avoided, and it was not until the applicants’ disclosures that a complete solution for 3D layer transfer over copper/aluminum was found.” Reply Br. 8. In the Appeal Brief, Appellants assert their claims “teach at least four methods to overcome the exfoliating ion-implant damage of the ion-cut process.” Appeal Br. 19. Notably, however, independent claims 13 and 46 recite only that “said transferring said first mono-crystalline layer comprises an ion-cut,” without any limitation to any details of that “complete solution” purported to overcome the alleged problems of the prior art or to the

⁵ Appellants state that they

have in-hand and can provide 1.132 declarations from non-Applicants, if asked for by the examiner/board, to document that even IBM’s 3DIC expert, IBM Fellow Dr. Subramanian S. Iyer in a 2013 telephone conversation, had this same view expressed by Lee...that ion-cut would create damages [sic] in single crystal silicon, the damages need high temperature to cure, and that high temperature would damage the aluminum/copper metallization underneath the ion-cut transferred layer...a technical feasibility concern.

Reply Br. 8. Appellants also assert that, “[w]hen told of the Applicant’s innovative solution, Dr. Iyer confirmed that it is a promising solution.” *Id.* Appellants have not made any such evidence of record in this appeal, however, and we accord Appellants’ attorney argument no weight. *See In re Geisler*, 116 F.3d 1465, 1471 (Fed. Cir. 1997) (attorney argument cannot take the place of evidence).

methods alleged “to overcome the exfoliating ion-implant damage.” *Id.*;
Reply Br. 8.

Appellants’ argument that high temperatures incompatible with aluminum or copper interconnects would be required to repair damage caused by Lee’s use of SmartCut is also unavailing. First, although Appellants cite certain high temperature annealing processes, we agree with the Examiner that a person of ordinary skill in the art would have known of common, alternative methods such as lower temperature anneals for longer times, polishing methods, and oxidation methods. Ans. 17. Moreover, even if high temperatures *were* required, the claims on appeal recite “providing a base wafer comprising a semiconductor substrate and a metal layer, said metal layer *comprising aluminum or copper.*” See claims 13, 46, 51 (italics added). As the Examiner points out, the use of the open-ended term “comprising” means that the metal layer is not limited to aluminum or copper, but merely must include some aluminum or copper. Ans. 18. Thus, as the Examiner also points out, the metal layer may be, for example, a tungsten-copper alloy having a melting point close to that of pure tungsten (i.e., 3422 °C), far in excess of the temperatures Appellants allege would be required to repair damage that may be caused by the SmartCut process. *Id.* at 18–19. As the Federal Circuit has explained, “[f]or a prior-art reference to be enabling, it need not enable the claim in its entirety, but instead the reference need only enable a single embodiment of the claim.” *In re Morsa*, 803 F.3d 1374, 1377 (Fed. Cir. 2015) (citing *Schering Corp. v. Geneva Pharm.*, 339 F.3d 1373, 1381 (Fed. Cir. 2003)).

For the foregoing reasons, we sustain the Examiner’s rejection of claims 13 and 46 under 35 U.S.C. § 102(b) as anticipated by Lee.

Claims 14, 39, 48, and 51

Claim 14 depends from claim 13 and further recites “wherein said first transistors are substantially horizontally orientated transistors.”

Claim 39 depends from claim 13 and further recites “wherein said first transistors comprise at least one FinFet transistor.” Claim 48 depends from claim 46 and further recites “wherein said second transistors comprise at least one FinFet transistor.” Claim 51 is an independent claim including the same limitations as independent claim 1 and dependent claim 39.

The Examiner finds Lee discloses “substantially horizontally orientated transistors,” as recited in claim 14 (Final Act. 4 (citing Lee ¶¶ 107, 109, 110)), and “FinFet transistor[s],” as recited in claims 39, 48, and 51 (*id.* at 4–7 (citing Lee ¶¶ 80, 105, Fig. 4D)). Appellants argue that FinFets are a type of horizontal transistor, and point to the Specification as explaining that “[t]hese transistors can be considered ‘planar transistors,’ meaning that current flow in the transistor channel is substantially in the horizontal direction.” Appeal Br. 20 (quoting Spec. ¶ 129). Appellants further argue that “[h]orizontal transistors formed over copper metallization is not taught or anticipated by Lee.” *Id.*

We agree with Appellants that neither FinFETs nor horizontal transistors are disclosed in the portions of Lee cited by the Examiner. Accordingly, we do not sustain the Examiner’s rejection of claims 14, 39, 48, and 51 under 35 U.S.C. § 102(b) as anticipated by Lee.

Claims 15 and 25

Claims 15 and 25 depend from claim 13 and recite “wherein said first transistors are recessed channel array transistors (‘RCAT’)” and “wherein said first transistors are trench MOSFET transistors,” respectively. The Examiner finds that Temmler teaches RCATs and MOSFETs and that claims 15 and 25 would have been obvious over the combination of Lee, as applied to claim 13, with Temmler. Final Act. 8. Citing Temmler, the Examiner finds that the motivation for such combination would have been to produce the predictable results of using a type of trench MOSFET that allows for optimization of channel length and performance. *Id.* (citing Temmler ¶¶ 5–6).

Appellants contend that Temmler does not remedy the deficiencies of Lee, and further, that “Temmler teaches 2D transistors with 3D channels, not monolithic 3D ICs” and that “whenever copper interconnect on the under layer is taught by Lee, Lee only creates vertical transistors,” whereas “RCAT transistors and trench MOSFETs are horizontal transistors.” Appeal Br. 21–22. Lastly, Appellants argue that “there is no suggestion to modify Lee and Temmler to arrive at the invention as claimed.” *Id.* at 22.

Appellants’ arguments are unpersuasive. First, for the reasons set forth in our discussion of claim 13 *supra*, we disagree with Appellants’ identification of alleged deficiencies in Lee. Second, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. *See In re Merck & Co., Inc.*, 800 F.2d 1091, 1097 (Fed. Cir. 1986); *In re Keller*, 642 F.2d 413, 426 (CCPA 1981). Here, the Examiner does not rely on Temmler for disclosure of “monolithic 3D ICs,” but only for its disclosure of RCAT transistors and trench

MOSFETs, which the Examiner recognizes are not taught by Lee. *See* Final Act. 8. Because the Examiner relies on Temmler, not Lee, as teaching RCATs and trench MOSFETs, Appellants' argument that Lee does not *also* teach those elements is unavailing. Lastly, we are persuaded that the Examiner has adequately provided "some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." *See KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007) (quoting *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006)).

Accordingly, we sustain the Examiner's rejection of claims 15 and 25 under 35 U.S.C. § 103(a) for obviousness over the combination of Lee and Temmler.

Claim 16

Claim 16 depends from claim 13 and further recites "wherein said first transistors are junction-less transistors."

The Examiner finds Lee does not teach that the first transistors are junction-less but that Gill does so, and that it would have been obvious at the time the invention was made to add the invention of Gill to the invention of Lee. Final Act. 8–9.

In response, Appellants argue that "Gill teaches a diffusion-less transistor (wherein the source and drain are not within the body containing the channel, and are of opposite type with respect to the substrate/body), not a junction-less transistor (wherein the source and drain and channel all are of the same dopant type)." Appeal Br. 23 (citing Lilienfeld, U.S. Patent No. 1,745,175; Jean-Pierre Colinge et al., *Nanowire transistors without junctions*, 5 Nature Nanotechnology 225 (2010) ("Colinge")).

We agree with Appellants that neither Gill nor the combination of Lee and Gill teaches “junction-less transistors” as that term is used in the Specification. *See* Spec. ¶ 145 (citing Colinge). Accordingly, we do not sustain the Examiner’s rejection of claim 16 under 35 U.S.C. § 103(a) as obvious over Lee and Gill.

Claims 17, 47, and 52

Claims 17, 47, and 52 depend from claims 13, 46, and 51, respectively, and each further recite “wherein said . . . transistors comprise at least one p-type transistor and one n-type transistor.” The Examiner finds that Gonzalez teaches these additional limitations not taught by Lee and that it would have been obvious to one of ordinary skill in the art to combine the inventions of Gonzalez and Lee. Final Act. 9 (citing Gonzalez ¶ 55). The Examiner finds motivation for such combination in Gonzalez, namely to “produce[] the predictable results of forming both PMOS and NMOS devices, such as for devices such as CMOS that require both P and N type transistors.” *Id.* (citing Gonzalez ¶ 55).

Appellants contend that Gonzalez does not remedy the deficiencies of Lee, and further, that

Gonzalez teaches n and p transistors on the second layer formed by implantation and activation (high temperatures) after forming semiconductor material base 102 (the second layer) and with no copper between the two stacked semiconductor layers (uses high temperature connections[. . .]silicon, etc., or metal connections after second layer transistors are formed), which would not work in the presence of copper metallization between the two layers. Lee does not teach how to form n and p on the same semiconductor layer, that one semiconductor layer being above copper metallization.

Appeal Br. 24–25. Lastly, Appellants argue that “there is no suggestion to modify Lee and Gonzalez to arrive at the invention as claimed.” *Id.* at 25.

Appellants’ arguments are unpersuasive as to claims 17 and 47. First, for the reasons set forth in our discussion of claims 13 and 46 *supra*, we disagree with Appellants’ identification of alleged deficiencies in Lee with respect to those claims. Second, Appellants provide no evidence in support of their argument that Gonzalez’s teachings would not work in the presence of copper metallization. Indeed, as also explained in our discussion of claims 13 and 46, the use of the open-ended phrase “said metal layer comprising aluminum or copper” renders each of the independent claims and claims dependent from them broader than simply to require “copper metallization.” In any event, we do not understand the Examiner to suggest wholesale incorporation of Gonzalez’s formation of transistors by implantation and activation into Lee, as suggested by Appellants, as the Examiner finds Lee itself teaches the claim 13 step of “processing said first mono-crystalline layer to define first transistors.” *See Keller*, 642 F.2d at 425 (“The test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference.” (citations omitted)); *see also id.* at 426 (explaining that one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references). Lastly, we are persuaded that the Examiner has adequately provided “some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.” *See KSR*, 550 U.S. at 418 (citation omitted).

As explained in our discussion of claim 51 *supra*, we agree with Appellants that Lee does not teach the limitation “wherein said first

transistors comprise at least one FinFet transistor.” Because claim 52 also includes that limitation by virtue of its dependency from claim 51, and because the Examiner does not cite Gonzalez as teaching a FinFET transistor, we do not sustain the Examiner’s rejection of claim 52 over the combination of Lee and Gonzalez.

Accordingly, we sustain the Examiner’s rejection of claims 17 and 47 under 35 U.S.C. § 103(a) for obviousness over the combination of Lee and Gonzalez, but do not sustain the Examiner’s rejection of claim 52 over that same combination.

Claim 20

Claim 20 depends from claim 13 and further recites “wherein said semiconductor substrate comprises alignment marks and said first transistors are defined in alignment with said alignment marks.” The Examiner finds that Yu teaches these additional limitations not taught by Lee and that it would have been obvious to one of ordinary skill in the art to combine the inventions of Yu and Lee. Final Act. 10 (citing Yu ¶ 32, Fig. 2K). The Examiner finds motivation for such combination in Yu, namely to “produce[] the predictable results of forming predefined regions for use in aligning features in stacked substrates to each other.” *Id.* (citing Yu ¶ 32).

Appellants contend that Yu does not remedy the deficiencies of Lee and that “there is no suggestion to modify Lee and Yu to arrive at the invention as claimed.” Appeal Br. 26.

Appellants’ arguments are unpersuasive. For the reasons set forth in our discussion of claim 13 *supra*, we disagree with Appellants’ identification of alleged deficiencies in Lee. Moreover, we are persuaded that the

Examiner has adequately provided “some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.” *See KSR*, 550 U.S. at 418 (citation omitted).

Accordingly, we sustain the Examiner’s rejection of claim 20 under 35 U.S.C. § 103(a) for obviousness over the combination of Lee and Yu.

Claim 21

Claim 21 depends from claim 13 and further recites “wherein at least one of said first transistors has a side gate.” The Examiner finds that Mukasa teaches this additional limitation not taught by Lee and that it would have been obvious to one of ordinary skill in the art to combine the inventions of Mukasa and Lee. Final Act. 10–11 (citing Mukasa ¶ 189). The Examiner finds motivation for such combination in Mukasa, namely to “produce[] the predictable results of using a transistor wherein the location of the gate with respect to insulators, source, and drain may be optimized for better performance.” *Id.* at 11 (citing Mukasa ¶¶ 189–193).

Appellants contend that Mukasa does not remedy the deficiencies of Lee and that “there is no suggestion to modify Lee and Mukasa to arrive at the invention as claimed.” Appeal Br. 27.

Appellants’ arguments are unpersuasive. For the reasons set forth in our discussion of claim 13 *supra*, we disagree with Appellants’ identification of alleged deficiencies in Lee. Moreover, we are persuaded that the Examiner has adequately provided “some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.” *See KSR*, 550 U.S. at 418 (citation omitted).

Accordingly, we sustain the Examiner's rejection of claim 21 under 35 U.S.C. § 103(a) for obviousness over the combination of Lee and Mukasa.

Claim 40

Claim 40 depends from claim 13 and further recites "wherein the ion-implantation of said ion-cut is from the backside of the wafer." The Examiner finds that Rayssac teaches this additional limitation not taught by Lee and that it would have been obvious to one of ordinary skill in the art to combine the inventions of Rayssac and Lee. Final Act. 11 (citing Rayssac, Fig. 3). The Examiner finds motivation for such combination in Rayssac, namely to "produce[] the predictable results of implanting from the side that is later removed, so any possible damage that would occur in that region due to the passage of the ions would not effect [sic] the final device." *Id.* (citing Rayssac, Figs. 4, 5).

Appellants contend that Rayssac does not remedy the deficiencies of Lee; that "Rayssac's backside implant would not work for forming 3D-IC transistors as taught by Lee as the transistors would be face down into the transferred substrate"; that "Rayssac has been public for many years and no one has combined Rayssac with Lee, etc.[,] until this (and related) application with additional and enabling innovation"; and that "there is no suggestion to modify Lee and Rayssac to arrive at the invention as claimed." Appeal Br. 28.

Appellants' arguments are unpersuasive. First, for the reasons set forth in our discussion of claim 13 *supra*, we disagree with Appellants' identification of alleged deficiencies in Lee. Second, Appellants provide no

evidence in support of their argument that Rayssac's teachings would not work for forming 3D-IC transistors. Third, it is well-established that "[a]bsent a showing of long-felt need or the failure of others, the mere passage of time without the claimed invention is not evidence of nonobviousness." *Iron Grip Barbell Co. v. USA Sports, Inc.*, 392 F.3d 1317, 1325 (Fed. Cir. 2004); *accord In re Kahn*, 441 F.3d 977, 990–91 (Fed. Cir. 2006). Consequently, the fact that no one may have combined Rayssac and Lee before is insufficient by itself to establish non-obviousness of the claimed invention. Finally, we are persuaded that the Examiner has adequately provided "some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." *See KSR*, 550 U.S. at 418 (citation omitted).

Accordingly, we sustain the Examiner's rejection of claim 40 under 35 U.S.C. § 103(a) for obviousness over the combination of Lee and Rayssac.

Claims 41, 44, 49, and 53

Claims 41, 49, and 53 depend from claims 13, 46, and 51, respectively, and each further recite "wherein an optical anneal is performed after said ion-cut to repair damage from said ion-cut." Claim 44 depends from claim 41 and further recites "wherein said optical anneal is performed by a laser." The Examiner finds that Yamazaki teaches these additional limitations not taught by Lee and that it would have been obvious to one of ordinary skill in the art to combine the inventions of Yamazaki and Lee. Final Act. 12 (citing Yamazaki ¶ 266). The Examiner finds motivation for such combination in Yamazaki, namely to "produce[] the predictable results

of repairing damage to a crystal structure caused by ion implantation.” *Id.* (citing Yamazaki ¶ 266).

Appellants contend that Yamazaki does not remedy the deficiencies of Lee; that “Yamazaki does not teach using laser anneal to repair damages when over copper metallization that needs to be undamaged by the anneal”; that “Yamazaki has been public for many years and no one has combined Yamasaki [sic] with Lee, etc.[,] until this (and related) application”; and that “there is no suggestion to modify Lee and Yamazaki to arrive at the invention as claimed.” Appeal Br. 30.

Appellants’ arguments are unpersuasive as to claims 41, 44, and 49. First, for the reasons set forth in our discussion of claims 13 and 46 *supra*, we disagree with Appellants’ identification of alleged deficiencies in Lee with respect to those claims. Second, because the rejection is based on the combination of Lee and Yamazaki, rather than on Yamazaki alone, Appellants’ argument that Yamazaki does not teach “copper metallization”—for which the Examiner relies on Lee—is unavailing. Appellants do not provide any evidence that Yamazaki’s use of laser annealing to repair damage is unsuitable for use with Lee’s copper metallization. Third, the fact that no one may have combined Yamazaki and Lee before is insufficient by itself to establish non-obviousness of the claimed invention. *See Kahn*, 441 F.3d at 990–91; *Iron Grip Barbell*, 392 F.3d at 1325. Finally, we are persuaded that the Examiner has adequately provided “some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.” *See KSR*, 550 U.S. at 418 (citation omitted).

As explained in our discussion of claim 51 *supra*, we agree with Appellants that Lee does not teach the limitation “wherein said first transistors comprise at least one FinFet transistor.” Because claim 53 also includes that limitation by virtue of its dependency from claim 51, and because the Examiner does not cite Yamazaki as teaching a FinFET transistor, we do not sustain the Examiner’s rejection of claim 53 over the combination of Lee and Yamazaki.

Accordingly, we sustain the Examiner’s rejection of claims 41, 44, and 49 under 35 U.S.C. § 103(a) for obviousness over the combination of Lee and Yamazaki, but do not sustain the Examiner’s rejection of claim 53 over that same combination.

Claims 42 and 43

Claim 42 depends from claim 13 and further recites “wherein an oxidation is performed after said ion-cut to repair damage from said ion-cut.” Claim 43 also depends from claim 13 and further recites “wherein a CMP process is performed after said ion-cut to repair damage from said ion-cut.” The Examiner finds that Kamiyama teaches these additional limitations not taught by Lee and that it would have been obvious to one of ordinary skill in the art to combine the inventions of Kamiyama and Lee. Final Act. 13 (citing Kamiyama ¶¶ 10, 89, Fig. 2). The Examiner finds motivation for such combination in Kamiyama, namely to “produce[] the predictable results of forming a smoother surface.” *Id.* (citing Kamiyama ¶ 94).

Appellants contend that Kamiyama does not remedy the deficiencies of Lee; that “Kamiyama teaches a flow with an 1100°C heat treatment for

two hours (Kamiyama [0081]), and a sacrificial oxidation at 850-1350°C (Kamiyama [0063]), both of which would be incompatible with the below 400°C process needs of the instant application claimed flow”; that “Kamiyama has been public for many years and no one has combined Kamiyama with Lee, etc. until this (and related) application with additional and enabling innovation”; and that “there is no suggestion to modify Lee and Kamiyama to arrive at the invention as claimed.” Appeal Br. 31.

Appellants’ arguments are unpersuasive. First, for the reasons set forth in our discussion of claim 13 *supra*, we disagree with Appellants’ identification of alleged deficiencies in Lee. Second, contrary to Appellants’ suggestion, claims 42 and 43 do not recite any limitation to “below 400°C” processes. *Contra* Appeal Br. 31. Third, the fact that no one may have combined Kamiyama and Lee before is insufficient by itself to establish non-obviousness of the claimed invention. *See Kahn*, 441 F.3d at 990–91; *Iron Grip Barbell*, 392 F.3d at 1325. Finally, we are persuaded that the Examiner has adequately provided “some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.” *See KSR*, 550 U.S. at 418 (citation omitted).

Accordingly, we sustain the Examiner’s rejection of claims 42 and 43 under 35 U.S.C. § 103(a) for obviousness over the combination of Lee and Kamiyama.

Claims 45, 50, and 54

Claims 45, 50, and 54 depend from claims 13, 46, and 51, respectively, and each recite “wherein said . . . transistors are high k metal gate (HKMG) transistors.” The Examiner finds that Ahn teaches this

additional limitation not taught by Lee and that it would have been obvious to one of ordinary skill in the art to combine the inventions of Ahn and Lee. Final Act. 13 (citing Ahn ¶ 5). The Examiner finds motivation for such combination in Ahn, namely to “produce[] the predictable results of forming a[] transistor out of a material that has a beneficial property to transistor performance, by allowing the use of high-reliability transistors by using thin dielectrics.” *Id.* at 14 (citing Ahn ¶ 5).

Appellants contend that Ahn does not remedy the deficiencies of Lee; that “Ahn, as well as Intel and others a few years before Ahn, have disclosed HKMG transistor technology yet Lee did not propose such in any application”; and that “there is no suggestion to modify Lee and Ahn to arrive at the invention as claimed.” Appeal Br. 33.

Appellants’ arguments are unpersuasive as to claims 45 and 50. First, for the reasons set forth in our discussion of claims 13 and 46 *supra*, we disagree with Appellants’ identification of alleged deficiencies in Lee with respect to those claims. Second, because the rejection is based on the combination of Lee and Ahn, rather than on Lee alone, Appellants’ argument that Lee did not propose the use of HKMG transistor technology is unavailing. Finally, we are persuaded that the Examiner has adequately provided “some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.” *See KSR*, 550 U.S. at 418 (citation omitted).

As explained in our discussion of claim 51 *supra*, we agree with Appellants that Lee does not teach the limitation “wherein said first transistors comprise at least one FinFet transistor.” Because claim 54 also includes that limitation by virtue of its dependency from claim 51, and

because the Examiner does not cite Ahn as teaching a FinFET transistor, we do not sustain the Examiner's rejection of claim 54 over the combination of Lee and Ahn.

Accordingly, we sustain the Examiner's rejection of claims 45 and 50 under 35 U.S.C. § 103(a) for obviousness over the combination of Lee and Ahn, but do not sustain the Examiner's rejection of claim 54 over that same combination.

NEW GROUNDS OF REJECTION PURSUANT TO 37 C.F.R. § 41.50(b)

Claims 14, 39, 48, and 51 are rejected on a new ground of rejection under 35 U.S.C. § 103(a) as unpatentable over Lee, as applied by the Examiner to claims 13 and 46, in view of Temmler. Lee teaches all limitations of claims 13 and 46, but does not expressly teach wherein said first transistors are substantially horizontally orientated transistors, as recited in claim 14; wherein said first transistors comprise at least one FinFet transistor, as recited in claims 39 and 51; or wherein said second transistors comprise at least one FinFet transistor, as recited in claim 48. Temmler teaches or suggests horizontally orientated transistors and FinFET transistors, because Temmler discloses 3D-channel field-effect transistors with a FinFET-like fully depleted channel section. Temmler ¶¶ 13, 14, 37, 38, Figs. 5A–5C, 6A–6C. It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate Temmler's transistors with a FinFET-like fully depleted channel section into the invention of Lee, in order to produce the predictable result of enhancing switching characteristics by forming a thin semiconductor fin that can be fully depleted. *See id.* ¶¶ 6, 37.

Claim 16 is rejected on a new ground of rejection under 35 U.S.C. § 103(a) as unpatentable over Lee, as applied by the Examiner to claim 13, in view of Applicant-Admitted Prior Art. Lee teaches all limitations of claim 13, but does not expressly teach wherein said first transistors are junction-less transistors, as recited in claim 16. Jean-Pierre Colinge et al., *Nanowire transistors without junctions*, 5 Nature Nanotechnology 225 (2010) (“Colinge”), cited at paragraph 145 of the Specification, teaches junctionless transistors and that “[h]aving no junctions presents a great advantage.” Colinge 225. It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the junction-less transistors described by Colinge into the invention of Lee, in order to avoid known severe limitations on the processing thermal budget, development of costly millisecond annealing techniques, and requirements for ultrasharp doping concentration gradients necessitated by switching from n-type to p-type doping within the small dimensions of modern transistors, thereby “allow[ing] one to fabricate devices with shorter channels” more efficiently. *Id.* at 225–26.

Claim 52 is rejected on a new ground of rejection under 35 U.S.C. § 103(a) as unpatentable over Lee and Temmler as applied to claim 51, in further view of Gonzalez. Lee and Temmler teach all the limitations of claim 51, but do not expressly teach wherein said first transistors comprise at least one p-type transistor and one n-type transistor, as recited in claim 52. Gonzalez teaches p-type and n-type transistors. Gonzalez ¶ 55. It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate Gonzalez’s p-type and n-type transistors into the

invention of Lee, in order to produce the predictable result of forming a CMOS structure including both PMOS and NMOS devices. *See id.*

Claim 53 is rejected on a new ground of rejection under 35 U.S.C. § 103(a) as unpatentable over Lee and Temmler as applied to claim 51, in further view of Yamazaki. Lee and Temmler teach all limitations of claim 51, but do not expressly teach wherein an optical anneal is performed after said ion-cut to repair damage from said ion-cut, as recited in claim 53. Yamazaki teaches repairing damage by performing an optical anneal, namely laser annealing. Yamazaki ¶ 266. It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate Yamazaki's optical anneal into the invention of Lee, in order to produce the predictable result of repairing damage caused by ion implantation. *See id.*

Claim 54 is rejected on a new ground of rejection under 35 U.S.C. § 103(a) as unpatentable over Lee and Temmler as applied to claim 51, in further view of Ahn. Lee and Temmler teach all limitations of claim 51, but do not expressly teach wherein said first transistors are high k metal gate (HKMG) transistors, as recited in claim 54. Ahn teaches high k metal gate (HKMG) transistors. Ahn ¶ 5. It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate Ahn's HKMG transistors into the invention of Lee, in order to produce the predictable result of forming a transistor out of a material that enhances the transistor performance and reliability by using thin dielectrics. *See id.*

DECISION

The Examiner's rejection of claims 13 and 46 under 35 U.S.C. § 102(b) is AFFIRMED.

The Examiner's rejection of claims 14, 39, 48, and 51 under 35 U.S.C. § 102(b) is REVERSED.

The Examiner's rejections of claims 15, 17, 20, 21, 25, 40–45, 47, 49, and 50 under 35 U.S.C. § 103(a) are AFFIRMED.

The Examiner's rejections of claims 16 and 52–54 under 35 U.S.C. § 103(a) are REVERSED.

In NEW GROUNDS OF REJECTION pursuant to our authority under 37 C.F.R. § 41.50(b), we reject claims 14, 39, 48, and 51 under 35 U.S.C. § 103(a) as being unpatentable over Lee and Temmler; we reject claim 16 under 35 U.S.C. § 103(a) as being unpatentable over Lee and Applicant-Admitted Prior Art; we reject claim 52 under 35 U.S.C. § 103(a) as being unpatentable over Lee, Temmler, and Gonzalez; we reject claim 53 under 35 U.S.C. § 103(a) as being unpatentable over Lee, Temmler, and Yamazaki; and we reject claim 54 under 35 U.S.C. § 103(a) as being unpatentable over Lee, Temmler, and Ahn.

TIME PERIOD FOR RESPONSE

This decision contains new grounds of rejection pursuant to 37 C.F.R. § 41.50(b). Section 41.50(b) provides “[a] new ground of rejection pursuant to this paragraph shall not be considered final for judicial review.”

Section 41.50(b) also provides:

When the Board enters such a non-final decision, the appellant, within two months from the date of the decision, must exercise one of the following two options with respect to the new ground

of rejection to avoid termination of the appeal as to the rejected claims:

(1) *Reopen prosecution.* Submit an appropriate amendment of the claims so rejected or new Evidence relating to the claims so rejected, or both, and have the matter reconsidered by the examiner, in which event the prosecution will be remanded to the examiner. The new ground of rejection is binding upon the examiner unless an amendment or new Evidence not previously of Record is made which, in the opinion of the examiner, overcomes the new ground of rejection designated in the decision. Should the examiner reject the claims, appellant may again appeal to the Board pursuant to this subpart.

(2) *Request rehearing.* Request that the proceeding be reheard under § 41.52 by the Board upon the same Record. The request for rehearing must address any new ground of rejection and state with particularity the points believed to have been misapprehended or overlooked in entering the new ground of rejection and also state all other grounds upon which rehearing is sought.

Further guidance on responding to new grounds of rejection can be found in MPEP § 1214.01 (9th ed., rev. 07.2015, Nov. 2015).

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a). *See* 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED-IN-PART; 37 C.F.R. § 41.50(b)