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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/583,552	08/21/2009	Steven Huynh	ACT-007-4C	7144

47713 7590 05/26/2015

IMPERIUM PATENT WORKS
P.O. BOX 607
Pleasanton, CA 94566

EXAMINER
SIEK, VUTHE

ART UNIT	PAPER NUMBER
2851	

MAIL DATE	DELIVERY MODE
05/26/2015	PAPER

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte STEVEN HUYNH and DAVID KUNST

Appeal 2013-006708
Application 12/583,552[1]
Technology Center 2800

Before CHUNG K. PAK, ROMULO H. DELMENDO, and BEVERLY A. FRANKLIN, *Administrative Patent Judges*.

DELMENDO, *Administrative Patent Judge*.

DECISION ON APPEAL

The Appellants seek our review under 35 U.S.C. § 134(a) of a decision of the Primary Examiner to reject claims 56–65. We have jurisdiction under 35 U.S.C. § 6.

We AFFIRM.

[1] The Appellants identify the real party in interest as "Active-Semi, Inc. (BVI)" (Appeal Brief filed December 2, 2012, hereinafter "App. Br.," 1).

BACKGROUND

The "invention relates to the design and layout of integrated circuits (ICs)" and, more specifically, "to a modular partition approach used to create extremely versatile high performance, application specific ICs in the shortest possible time frame" (Specification, hereinafter "Spec.," ¶ 2). Representative claim 56 is reproduced from page 7 of the Appeal Brief (Claims App'x) as follows:

> 56. A method of making an integrated circuit, comprising:
>
> specifying a first modular tile having a square shape, wherein the first modular tile performs a first function;
>
> specifying a second modular tile having a square shape of the same size as the first modular tile, wherein the second modular tile performs a second function, wherein each of the first modular tile and the second modular tile has a standardized set of connectors disposed at fixed locations on each of the four edges of each modular tile such that a first set of connectors on an edge of the first modular tile aligns with a second set of connectors on an edge of the second modular tile regardless of whether the second modular tile is disposed to the right, to the left, above, or below the first modular tile; and
>
> generating a physical layout for the integrated circuit such that an end application of the integrated circuit is operational when the first function and the second function are performed regardless of whether the second modular tile is disposed to the right, to the left, above, or below the first modular tile.

THE REJECTION

The Examiner rejected claims 56–65 under 35 U.S.C. § 101 as drawn to patent-ineligible abstract idea (Examiner's Answer entered February 27,

2013, hereinafter "Ans.," 2–4; Final Office Action entered November 26, 2012, hereinafter "Final Act.," at 2).[2]

DISCUSSION

The Appellants argue claims 56–65 together (App. Br. 3–6). Therefore, pursuant to 37 C.F.R. § 41.37(c)(1)(iv), we confine our discussion to claim 56, which we select as representative. Additionally, by operation of the rule, claims 57–65 stand or fall with claim 56.

The Examiner found that "the claimed method could encompass processes consisting entirely of mental steps and is thus merely an abstract idea" (Ans. 2). Based on this finding, the Examiner held that the claims are directed to patent-ineligible subject matter (*id*.).

The Appellants contend that the Examiner's rejection is flawed for three reasons. First, the Appellants contend that "claim 56 is tied to a machine, namely the integrated circuit that is made by specifying the recited tiles and by generating the recited physical layout" and, therefore, it satisfies the "machine-or-transformation" test (App. Br. 4). Second, the Appellants argue that even if claim 56 does not satisfy the "machine-or-transformation" test, it does not attempt to claim an abstract idea because it recites "concrete things such as an integrated circuit, connectors, an edge of a tile, and a physical layout for an integrated circuit" (*id*.). According to the Appellants, "[m]aking an integrated circuit by generating a physical layout is not a purely abstract mental process, but rather involves a physical object" (*id*. at 5). Third, the Appellants argue that the claims recite "statutory subject

[2] Claims 66–75 have been allowed (App. Br. 1; Final Act. 2).

matter because any abstract ideas recited in the claims are attached to a specific application, namely making an integrated circuit" (*id*.).

The Appellants' arguments—some of which overlap with one another—do not persuade us of any reversible error in the Examiner's rejection. *In re Jung*, 637 F.3d 1356, 1365 (Fed. Cir. 2011).

First, we disagree with the Appellants that claim 56 satisfies the "machine-or-transformation" test. *Bilski v. Kappos*, 561 U.S. 593, 594 (2010) ("The machine-or-transformation test is not the sole test for patent eligibility under § 101" but it "may be a useful and important clue or investigative tool").

Although claim 56 recites a method of making an integrated circuit comprising the steps of "specifying" the recited modular tiles and "generating a physical layout for the integrated circuit," we agree with the Examiner (Ans. 3) that the claimed method is not tied to a particular machine or apparatus. Nor does it transform an article to a different state or thing (*id*.). Rather, as correctly found by the Examiner (Final Act. 2), the claimed method can consist entirely of the mental steps of "specifying" the recited molecular tiles and "generating a physical layout for the integrated circuit" (Spec. ¶ 32) (explaining that the drawing represented by Fig. 3A is a "typical layout"). Contrary to the Appellants' belief (App. Br. 5), the "generating a physical layout for the integrated circuit such that . . ." step does not require the *manufacture* of an integrated circuit but merely the generation of a layout (i.e., the generation of a design drawing of a circuit). Absent further steps that are positively recited to require actual manufacturing of the integrated circuit, we find no error in the Examiner's

determination that the claimed method attempts to cover an abstract idea in violation of 35 U.S.C. § 101.

To the extent that the preamble language "method of making an integrated circuit" might be construed to necessarily require manufacturing steps, the Appellants themselves indicate that the "tile modules are used to specify and form the IC in a *standard* IC fabrication process" (Spec. ¶ 9) (emphasis added). Thus, the claimed method is nothing more than a drafting effort to monopolize the abstract idea of specifying and generating a design for the integrated circuit. *Alice Corp. Pty. Ltd. v. CLS Bank Intern.*, 134 S. Ct. 2347, 2357 (2014) ("'Simply appending conventional steps, specified at a high level of generality,' was not '*enough*'. . . .") (internal citation omitted).

For these reasons, and those given by the Examiner, we uphold the rejection of claim 56.

SUMMARY

The Examiner's rejection under 35 U.S.C. § 101 of claims 56–65 as drawn to patent-ineligible subject matter is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1).

AFFIRMED

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