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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex Parte MARTIM CARBONE, BERNHARD JANSEN, HARIGOVIND V. RAMASAMY, MATTHIAS SCHUNTER, AXEL TANNER, and DIEGO M. ZAMBONI

Appeal 2013-006276
Application 12/022,184[1]
Technology Center 2100

Before ST. JOHN COURTENAY III, THU A. DANG, and LARRY J. HUME, *Administrative Patent Judges*.

HUME, *Administrative Patent Judge*.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134(a) of the final rejection of claims 1–29. We have jurisdiction under 35 U.S.C. § 6(b).

We AFFIRM-IN-PART.

[1] According to Appellants, the real party in interest is International Business Machines Corp. App. Br. 2.

STATEMENT OF THE CASE[2]

The Invention

Appellants' claimed invention relates to "hardware emulation using on-the-fly virtualization." Title.

Exemplary Claim

Claim 1, reproduced below, is representative of the subject matter on appeal (lettering and *emphasis* added to contested limitations):

> 1. A method for addressing at least one anomaly associated with at least one actual hardware element in a computer system having a plurality of hardware elements, said method comprising the steps of:
>
> [a] *responsive to detecting said at least one anomaly, inserting a virtualization layer between (i) an operating system of said computer system, and (ii) said plurality of hardware elements*; and
>
> [b] *performing at least one of hardware emulation and hardware deactivation on said at least one actual hardware element, with said virtualization layer*;
>
> [c] wherein *said insertion of said virtualization layer is accomplished in an on-the-fly manner*.

[2] Our decision relies upon Appellants' Appeal Brief ("App. Br.," filed Dec. 12, 2012); Reply Brief ("Reply Br.," filed Apr. 12, 2013); Examiner's Answer ("Ans.," mailed Mar. 19, 2013); Final Office Action ("Final Act.," mailed June 6, 2012); and the original Specification ("Spec.," filed Jan. 30, 2008).

Prior Art

The Examiner relies upon the following prior art as evidence in rejecting the claims on appeal:

Wolin et al. ("Wolin") US 6,661,203 B2 Dec. 9, 2003

Sami Vaarala, *Security Considerations of Commodityx86 Virtualization* (May 22, 2006) (Licentiate Thesis, Helsinki University of Technology (on file with Helsinki University)) (hereinafter "Vaarala").

Rejections on Appeal[3]

R1. Claims 1–14 and 16–29 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Vaarala. Final Act. 3.

R2. Claim 15 stands rejected under 35 U.S.C § 103(a) as being obvious over the combination of Vaarala and Wolin. Final Act. 11.

[3] In the event of further prosecution, we direct the Examiner's attention to a recent precedential Board decision to ensure that "computer program product" claims 20–22 and 28 are directed to statutory subject matter under § 101. Under our jurisprudence, the scope of the recited "computer usable readable recordable storage medium" appears to encompass transitory media such as signals or carrier waves. *See Ex parte Mewherter*, 107 USPQ2d 1857 (PTAB 2013) (precedential) (holding recited machine-readable storage medium ineligible under § 101 since it encompasses transitory media). Here, the recited "computer usable readable recordable storage medium" (claims 20–22 and 28) is not claimed as non-transitory, and the originally-filed Specification does not expressly and unambiguously disclaim transitory forms, such as signals, via a definition. "The medium can be an electronic, magnetic, optical, electromagnetic, infrared, or semiconductor system (or apparatus or device) *or a propagation medium*." Spec. 9, ll. 29–30 (emphasis added). Therefore, the "computer program product" of claims 20–22 and 28 is not limited to non-transitory forms and appears ineligible under § 101.

CLAIM GROUPING

Based on Appellants' arguments (App. Br. 16–22), we decide the appeal of Rejection R1 of independent claims 1, 16, 20 and 23 on the basis of representative claim 1; and we decide the appeal of Rejection R1 of claims 26–29 on the basis of representative claim 26. We decide the appeal of Rejection R1 of dependent claims 5–12, separately, *infra*, and we address Rejection R1 of dependent claims 2–4, 13, 14, 17–19, 21, 22, 24, and 25, not argued separately, *infra*. We address Rejection R2 of claim 15, not argued separately, *infra*.

Dependent claims not argued separately fall with the respective independent claim from which they depend. *See* 37 C.F.R. § 41.37(c)(1)(iv)(2012).

ISSUES AND ANALYSIS

In reaching this decision, we consider all evidence presented and all arguments actually made by Appellants. We do not consider arguments which Appellants could have made but chose not to make in the Briefs so that we deem any such arguments as waived. 37 C.F.R. § 41.37(c)(1)(iv).

We have reviewed the Examiner's rejections in light of Appellants' arguments. We agree with Appellants' arguments with respect to Rejection R1 of claims 5–12. However, we disagree with Appellants' arguments with respect to Rejection R1 of claims 1–4, 13, 14, and 16–29, as well as rejection R2 of claim 15. Thus, regarding claims 1–4, and 13–29, we incorporate herein and adopt as our own: (1) the findings and reasons set forth by the Examiner in the action from which this appeal is taken, and (2) the reasons and rebuttals set forth in the Examiner's Answer in response

to Appellants' arguments. We incorporate such findings, reasons, and rebuttals herein by reference unless otherwise noted. However, we highlight and address specific findings and arguments regarding the issues below for emphasis as follows.

1. Rejection R1: § 102(b) – Claims 1, 16, 20, and 23

Issue 1

Appellants argue (App. Br.16–19; Reply Br.4–5) the Examiner's rejection of independent claim 1 under 35 U.S.C. § 102(b) as being anticipated by Vaarala is in error. These contentions present us with the following issue:

Did the Examiner err in rejecting claim 1 under § 102 because the cited prior art does not disclose a method that includes contested limitations [a], [b], and [c], as recited in claim 1?

Analysis

Limitation [a]

Appellants first argue the Examiner's rejection is in error because the cited prior art does not disclose all limitations of claim 1 (App. Br. 16) and, in particular, contend Vaarala does not disclose the contested limitation [b] of claim 1. App. Br. 16. According to Appellants, Vaarala is deficient because a virtualization layer already exists in Vaarala and, therefore, there is no need to insert a virtualization layer. Appellants also argue the virtualization layer is not "Xen2," as the Examiner finds, but instead is "control domain 0," which allegedly is not a horizontal layer between the OS

layer and the hardware layer. Appellants further argue restarting a domain is not equivalent to inserting a virtualization layer.

Appellants contend:

> The Examiner asserts that page 56, FIG. 9, Xen 2 teaches inserting a virtualization layer *between* (i) an operating system of said computer system, and (ii) said plurality of hardware elements. In Fig. 9 and the corresponding discussion on page 55, Vaarala teaches that a control domain 0 provides virtualization management. Significantly, control domain 0 is illustrated *vertically* in FIG. 9, and is therefore *not a* horizontal layer *between* the OS (kernel) layer and the Hardware layer, comprised of CPUs, memory, network interfaces, etc. . . . Finally, FIG. 9 does not teach *any* virtualization *between* the horizontal OS (kernel) layer and the Hardware layer.

App. Br. 16–17. Further,

> Appellants submit that page 55 of Vaarala notes that the *domain can be restarted* when a failure is detected, which is *not* equivalent to *inserting a virtualization layer*.

Reply Br. 4.

However, we agree with the Examiner's finding that Vaarala discloses Appellants' claimed limitation [a] "responsive to detecting said at least one anomaly, inserting a virtualization layer between (i) an operating system of said computer system, and (ii) said plurality of hardware elements," as recited in claim 1. Ans. 3–4; Final Act. 3. We are not persuaded by Appellants' arguments because the Appellants do not address or rebut Examiner's specific mapping of Xen 2 to the virtualization layer. App. Br. 16–17; Ans. 4.

In particular, we agree with the Examiner's finding Vaarala's Xen 2 (Vaarala p. 56, Fig. 9) discloses a "virtualization layer," shown inserted

horizontally between Vaarala's Hardware layer ("plurality of hardware elements") and OS/Guest Kernel layers ("an operating system") and across all the domains, including control domain (domain 0) and trusted driver domain. Ans. 3–4, Final Act. 3. We find "Xen" is a hypervisor for virtualization and implements virtualization, whereas control domain 0 manages virtualization policy. Vaarala 52–53.

We also agree with the Examiner's finding, upon detecting a driver failure, the system restarts the trusted driver domain and repairs the failure by virtualizing the failed hardware. Ans. 3 (citing Vaarala at 55). We agree with the Examiner's finding that restarting with a virtualized environment discloses "inserting a virtualization layer" because, together with the restarting of the trusted driver domain, the Xen 2 "virtualization layer" implements the virtualization of the failed hardware. Ans. 3 (citing Vaarala at 55).

Accordingly, we agree with the Examiner and find the cited prior art discloses contested limitation [a] of claim 1.

Limitation [b]

Appellants contend:

> As previously indicated, Vaarala does *not* disclose or suggest *inserting a virtualization layer* between an operating system and hardware elements. Thus, Vaarala cannot disclose or suggest hardware emulation or deactivation on an actual hardware element ***with*** *the virtualization layer*.

App. Br. 18.

In particular, Appellants argue contested claim limitation [b] "performing at least one of hardware emulation and hardware deactivation

on said at least one actual hardware element, with said virtualization layer" is not met because Vaarala does not disclose inserting a virtualization layer.

However, as explained in the preceding analysis, which similarly applies here, we agree with the Examiner that the cited reference discloses, "inserting a virtualization layer." Therefore, we are unpersuaded by Appellants' contentions and find this limitation is anticipated by the cited reference.

Limitation [c]

Limitation [c] recites, in pertinent part, "wherein *said insertion of said virtualization layer is accomplished in an on-the-fly manner*" (emphasis added).

Appellants contend:

> [T]he Examiner asserts that Vaarala teaches that, "if processor capabilities change on-the-fly and the new processor does not support the extensions in question, the extensions must either be virtualized (if possible) . . ." Applicants note that virtualizing processor extensions is *not* equivalent to *inserting a virtualization layer responsive to detecting an anomaly and in an on the-fly manner*. Importantly, the above passage describes *processor capabilities* changing on-the-fly. The passage does not disclose or suggest *virtualizing* the extensions on-the-fly. No time frame is provided for *virtualizing* the extensions.

App. Br. 18–19.

Appellants define the claim limitation "on-the-fly manner" as "without rebooting the computer system." Spec. 1, ll. 30–31. Appellants further state "the virtualization layer can be installed on the fly" and explain that such an on-the-fly installation technique is already known in the prior art. Spec. 3–4 ("In the prior art, so-called "Hyperjacking" techniques have been used to

insert a software layer in a running system, for purposes of intrusion detection, without the need to reboot.").

However, we are not persuaded by Applicants' contentions, at least because Applicants admit this on-the-fly technique is conventionally known in the prior art to insert a software layer.

Furthermore, we agree with the Examiner's finding Xen 2's virtualization of processors, by implementing the desired emulation logic, can be performed "on the fly" (Ans. 3, citing Vaarala, pgs. 16, 2.2.3 (on the fly / just in time emulation), 24 (if processor capabilities change on-the-fly) Therefore, Xen 2 discloses "on the fly" insertion of a virtualization layer, thus meeting the limitation.

We also agree with Examiner's finding "on-the-fly is shown with respect to recovery from Ethernet interface driver failure where upon detecting the system restarted the domain and thus repaired the failure in 275 milliseconds" also discloses the contested "on-the-fly" limitation. Ans. 3, citing Vaarala at 55.

Based upon the findings above, on this record, we are not persuaded of error in the Examiner's reliance on the cited prior art to disclose the disputed limitations of claim 1, nor do we find error in the Examiner's resulting legal finding of anticipation.

Accordingly, Appellants have not provided sufficient evidence or argument to persuade us of any reversible error in the Examiner's reading of the contested limitations on the cited prior art. Therefore, we sustain the Examiner's anticipation rejection of independent claim 1 and claims 16, 20, and 23 which fall therewith. *See* Claim Grouping, *supra*.

2. Rejection R1: § 102(b) – Dependent Claims 5–12

Issue 2:

Appellants contend (App. Br.19–21; Reply Br.5–6) the Examiner's rejection of dependent claims 5–12 under 35 U.S.C. § 102(b) as being anticipated by Vaarala is in error. These contentions present us with the following issue:

Did the Examiner err in making the § 102 rejection over Vaarala by failing to provide a mapping of all the limitations of dependent claims 5–12 onto the reference in a manner adequate to establish a prima facie case of anticipation under 35 U.S.C. § 132?

Analysis

The Examiner states: "Appellants have provided no specific arguments regarding the dependent claims other than to say the prior art does not teach. As such the Examiner has no specific arguments to respond to and therefore the prior art rejection of these claims is MAINTAINED." Ans. 4.

Appellants contend:

> For dependent claims 5-12, the Examiner has cited to the same portion of Vaarala (page 26-27, Section 2.5.3), and has merely restated the claim language. In response, Appellants argued that pages 26-27 and section 2.5.3 of Vaarala generally address differences between physical and machine memory, memory management, indexed disk blocks and mapping, and are completely silent regarding: (1) determining whether data has been transferred from an original first storage element to a second storage element, and reading from the appropriate storage element based on the determination, (2) writing to a different storage element than that specified in a write request,

> (3) monitoring for completeness of a data migration between storage elements, and (4) responsive to the results of the monitoring, replacing a storage element or uninstalling a virtualization layer, as essentially recited in claims 5-12.
>
> Section 2.5.3 generally relates to the virtualization of storage resources, explaining how data is accessed, transferred and storage mapping. However, there is no specific disclosure in the cited portion that supports at least the above four (4) points, and the Examiner has not specifically tied any of the claim language of claims 5-12 to the cited reference.

Reply Br. 5–6, *See also* App. Br. 19–20.

We find Examiner has not articulated an analysis or mapping of any of dependent claims 5–12 on appeal, other than a repeated citation to pages 26–27, Section 2.5.3 of Vaarala for each one of these claims. Final Act. 4–6. We also find the Examiner has not adequately responded to Appellants' contentions in the Appeal Brief regarding these claims. Ans. 4.[4]

The Federal Circuit has held, "the prima facie case is merely a procedural device that enables an appropriate shift of the burden of production." *Hyatt v. Dudas*, 492 F.3d 1365, 1369 (Fed. Cir. 2007). The Federal Circuit stated this burden is met by "adequately explain[ing] the shortcomings it perceives so that the applicant is properly notified and able to respond." *Id.* at 1370. It is only "when a rejection is so uninformative that it prevents the applicant from recognizing and seeking to counter the grounds for rejection" that the prima facie burden has not been met and the rejection violates the minimal requirements of 35 U.S.C. § 132. *Chester v. Miller*, 906 F.2d 1574, 1578 (Fed. Cir. 1990). We find the Examiner has not

[4] In the Final Action, the Examiner merely repeats the claim language for each of claims 5–12, and asserts Vaarala generally discloses each of the limitations at pages 26–27, Section 2.5.3. Final Act. 4–6.

met his burden in establishing a prima facie case of anticipation of claims 5–12.

We would have to resort to conjecture to map the various limitations of the eight dependent claims to the Vaarala reference. Such conjecture on our part as to which reference teachings apply to which claims would impermissibly require us to resort to speculation, unfounded assumptions, and/or hindsight reconstruction. *See In re Warner*, 379 F.2d 1011, 1017 (CCPA 1967). "The review authorized by 35 U.S.C. Section 134 is not a process whereby the examiner . . . invite[s] the [B]oard to examine the application and resolve patentability in the first instance." *Ex parte Braeken*, 54 USPQ2d 1110, 1112 (BPAI 1999). We decline to engage in such speculation, unfounded assumptions, or hindsight reconstruction to make up for the deficiency in the Examiner's rejection which fails to set forth a prima facie case of anticipation for claims 5–12 pursuant to the requirements of § 132.

Accordingly, on this record, we cannot sustain the Examiner's anticipation rejection of claims 5–12 under §102(b).

3. Rejection R1: § 102(b) – Claims 26–29

Issue 3

Appellants contend (App. Br. 21–22; Reply Br.6) the Examiner erred in rejecting claim 26 under 35 U.S.C. § 102(b) as being anticipated by Vaarala. These contentions present us with the following issue:

Did the Examiner err in rejecting claim 26 under § 102(b), because the cited prior art does not disclose the contested limitation of claim 26, i.e.,

"said inserted virtualization layer interfaces directly to one or more of said plurality of hardware elements"?

Analysis

Appellants contend:

> Regarding claims 26-29, the Examiner asserts that Vaarala discloses wherein said inserted virtualization layer interfaces directly to one or more of said plurality of hardware elements (FIG. 8 where the Xen layer, which corresponds to the virtualization layer is directly connected to the physical CPU, memory, network interfaces and disks which reads on the hardware elements). As clearly shown in FIG. 8, however, it is the Hardware *device drivers* within Xen 1 of Vaarala that directly interface with the hardware. While the Xen layer may have some virtual components, the device drivers are not virtualized.

App. Br. 21–22. Appellants further contend:

> In contrast to what is claimed, the hardware device drivers in Fig. 8 of Vaarala are not hardware elements of the computer system (CPU in Fig. 8). Therefore, Vaarala fails to disclose an inserted virtualization layer that interfaces directly to one or more of said plurality of hardware elements (of the computer system).

Reply Br. 6.

However, the Examiner finds device drivers interfacing with Xen represent a virtual connection between virtual hardware and physical hardware, as shown in Figure 8. Vaarala, p. 53, Fig. 8 (reproduced below).

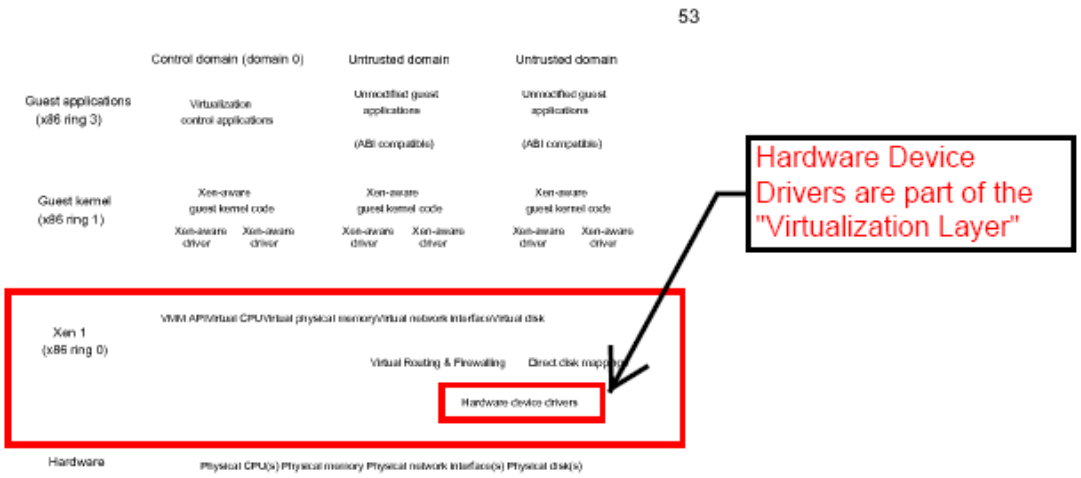

Figure8: Xen 1 Architecture

Figure 8 of Vaarala (annotated) illustrates the Xen 1 Architecture.

The Examiner also concludes the contested "inserted virtualization layer" limitation does not preclude inclusion of Vaarala's hardware device drivers within the virtualization layer to interface with the claimed "plurality of hardware elements." Ans. 4–5.

We agree with Examiner's findings and conclusions because Vaarala's Xen 1 ("virtualization layer"), including hardware device drivers, interfaces directly with the Hardware layer, which includes *physical* CPU's, memory, and disks, accessed via the interfaces through the hardware device drivers in the Xen 1 layer to the "plurality of hardware elements" in the hardware layer. Vaarala at 53, Fig. 8.

We note, "[d]uring prosecution . . . the PTO gives claims their 'broadest reasonable interpretation.'" *In re Bigio*, 381 F.3d 1320, 1324 (Fed. Cir. 2004) (quoting *In re Hyatt*, 211 F.3d 1367, 1372 (Fed. Cir. 2000)). We find the broadest reasonable interpretation of common claim element "hardware" does not exclude such hardware disclosed in Fig. 8 of the cited

reference, nor does the broadest reasonable interpretation of "virtualization layer" preclude the inclusion of hardware device drivers in such a layer.

Therefore, we are not persuaded by Appellants' contentions because they are inconsistent both internally and with Vaarala's disclosure, and do not overcome Examiner's specific findings.

Accordingly, we agree with Examiner and find the cited prior art discloses the contested limitation of claim 26, and claims 27–29 which fall therewith. *See* Claim Grouping, *supra*.

4. Rejection R1: § 102(b) – Claims 2–4, 13, 14, 17–19, 21, 22, 24, 25

In view of the lack of any substantive or separate arguments directed to anticipation Rejection R1 of claims 2–4, 13, 14, 17–19, 21, 22, 24, and 25 under § 102(b) (*see* App. Br. 22) [5], we sustain the Examiner's rejection of these claims, as they fall with representative independent claim 1. When Appellants do not separately argue the patentability of dependent claims, the claims stand or fall with the claims from which they depend. *See* 37 C.F.R. § 41.37(c)(1)(iv)(2012).

Accordingly, we sustain Rejection R1 of claims 2–4, 13, 14, 17–19, 21, 22, 24, and 25.

[5] Appellants merely argue these claims are patentable by virtue of their dependence on purportedly allowable independent claims 1, 16, 20, and 23. App. Br. 22.

5. Rejection R2: § 103(a) – Dependent Claim 15

In view of the lack of any substantive or separate arguments directed to obviousness Rejection R2 of claim 15 under § 103 (*see* App. Br. 22),[6] we sustain the Examiner's rejection of this claim, as it falls with independent claim 1. Arguments not made are waived. *See* 37 C.F.R. § 41.37(c)(1)(iv).

REPLY BRIEF

To the extent Appellants may advance new arguments in the Reply Brief (Reply Br. 4–6) not in response to a shift in the Examiner's position in the Answer, we note arguments raised in a reply brief, that were not raised in the appeal brief or are not responsive to arguments raised in the Examiner's Answer, will not be considered except for good cause. *See* 37 C.F.R. § 41.41(b)(2).

CONCLUSIONS

(1) The Examiner did not err with respect to anticipation Rejection R1 of claims 1–4, 13, 14, and 16–29 under 35 U.S.C. § 102(b) over the cited prior art of record, and we sustain the rejection.

(2) The Examiner erred with respect to anticipation Rejection R1 of claims 5–12 under 35 U.S.C. § 102(b) over the cited prior art of record, and we do not sustain the rejection.

(3) The Examiner did not err with respect to obviousness Rejection R2 of claim 15 under 35 U.S.C. § 103(a) over the cited prior art combination of record, and we sustain the rejection.

[6] Appellants merely argue this claim is patentable by virtue of its dependence on purportedly allowable claim 1. App. Br. 22.

DECISION

We affirm the Examiner's decision rejecting claims 1–4 and 13–29. We reverse the Examiner's decision rejecting claims 5–12.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv) (2011).

AFFIRMED-IN-PART

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