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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/275,091	12/09/2005	Robert J. Devins	BUR920050146US1	1121

44152 7590 01/23/2015

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ART UNIT	PAPER NUMBER
2447	

NOTIFICATION DATE	DELIVERY MODE
01/23/2015	ELECTRONIC

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte ROBERT J. DEVINS, DAVID W. MILTON, and PASCAL A. NSAME

Appeal 2012-009057
Application 11/275,091
Technology Center 2400

Before MAHSHID D. SAADAT, JOHN A. EVANS, and JOHN F. HORVATH, *Administrative Patent Judges*.

HORVATH, *Administrative Patent Judge*.

DECISION ON APPEAL

STATEMENT OF THE CASE

Appellants seek review of the Examiner's rejection of claims 1–12 and 22–43 under 35 U.S.C. § 134.[1] We have jurisdiction under 35 U.S.C. § 6(b).

We AFFIRM-IN-PART.

SUMMARY OF THE INVENTION

The invention is directed to a method of communicating or transferring data between multiple peer processors in a system-on-chip ("SoC") design verification environment. Spec. 9.

Claim 1, reproduced below, is illustrative of the claimed subject matter:

> 1. A method comprising:
>
> transferring data from a first processor to at least one pulse generator directly connected to an interrupt control of at least a second processor, the transferring of the data bypasses memory; and
>
> reading the transferred data directly from the at least one pulse generator by the at least a second processor.

REJECTIONS

Claim 35 stands rejected under 35 U.S.C § 101 as directed to non-statutory subject matter. Ans. 5.

Claims 1–12 and 22–43 stand rejected under 35 U.S.C § 103(a) as unpatentable over Lakhat,[2] Ward,[3] and Andrews.[4] Ans. 5.

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[1] Appellants only requested review of claims 1, 3–10 and 22–43. App. Br. 5. However, claims 1–12 and 22–43 stand rejected, Ans. 5, and Appellants have argued for the patentability of these claims. App. Br. 7–69. We therefore treat Appellants' request as a request to review the rejection of claims 1–12 and 22–43.

ISSUES AND ANALYSIS

I. Whether Lakhat's command register is a pulse generator recited in claim 1.

In rejecting claim 1, the Examiner finds Lakhat's command register 94 is a pulse generator directly connected to the interrupt control of NMP processor 32, and that NMP processor 32 reads data from command register 94. Ans. 6 (citing Lakhat 3:44–47). Appellants argue Lakhat's command register 94 is not a pulse generator because Lakhat does not disclose it generates a pulse, and "fails to even mention the claimed terms 'pulse' and 'generator' in the entirety of its disclosure." App. Br. 10. Moreover, Appellants argue "one of ordinary skill in the art would recognize that a register cannot correspond to a pulse generator," citing a description of a hardware register from Wikipedia. *Id*. We are not persuaded by Appellants' argument.

First, we are not persuaded by Appellants' argument that a person of ordinary skill in the art would recognize a register cannot correspond to a pulse generator. App. Br. 10. To the contrary, the Wikipedia article cited by Appellants in support of this proposition identifies a strobe register as one type of register, and indicates "a strobe register bit that *generates a one cycle pulse* into specialized hardware will always read logic 0." Wikipedia, http://en.wikipedia.org/wiki/Hardware_register (emphasis added). The

[2] U.S. Patent No. 6,154,785 issued Nov. 28, 2000
[3] U.S. Patent No. 6,937,611 B1 issued Aug. 30, 2005
[4] U.S. Patent No. 7,664,928 B1 issued Feb. 16, 2010

article further indicates one function of registers is to "*transmit to* or accept information from other registers." *Id*. (emphasis added).

Second, Appellants do not identify, nor do we find, a definition for a "pulse generator" in the Specification. Instead, Appellants direct us to another Wikipedia article, and claim the definition provided therein is the meaning the term would have had to a person of ordinary skill in the art. App. Br. 10. Wikipedia defines a pulse generator as "an electronic circuit *or* a piece of electronic test equipment used to generate rectangular pulses." Wikipedia, http://en.wikipedia.org/wiki/Pulse_generator. We accept Appellants' proposed definition of a "pulse generator," and adopt it as our own. We also note a person of ordinary skill in the art at the time of Appellants' invention would have also understood the following terms to have the following meanings:

1) Register: "A device capable of retaining information, often that contained in a small subset (for example, one word), of the aggregate information in a digital computer." *IEEE 100 The Authoritative Dictionary of IEEE Standards Terms* 949 (7th Ed. 2000);
2) Bus: "One or more conductors used for transmitting signals or power from one or more sources to one or more destinations." *Id*. at 128;
3) Signal: "A measureable quantity (e.g., a voltage) which varies in time in order to transmit information. . . . It is interpreted as a sequence of bits. . . . Signals are generated by a link output and are absorbed by a link input." *Id*. at 1047; and

4) Pulse: "A variation in the value of a magnitude which is short in relation to the time schedule of interest, the final value being the same as the initial value. Note: In digital logic circuits, a pulse is usually a voltage." *Id.* at 886.

The Examiner finds Lakhat teaches NMP processor 32 reads data from command register 94 through bus 15. Ans. 6 (citing Lakhat 3:44–47, Fig. 3). A person of ordinary skill in the art at the time of Appellants' invention would have understood this teaching to require command register 94 (the source) to transmit a signal (e.g., a voltage varying between high and low values) to NMP processor 32 (the destination) over bus 15. *See, e.g., IEEE Dictionary* at 128, 949, and 1047 (definitions of "bus," "signal," and "register"). A person of ordinary skill in the art at the time of Appellants' invention would also have understood that a voltage varying between high and low values would represent one or more pulses, and therefore that command register 94 was a pulse generator, as the Examiner correctly found. *Id*. at 886 (definition of "pulse"). Consequently, we sustain the Examiner's rejection of claim 1.

Appellants do not separately argue for the patentability of claims 2–4, 7, 9, 11, and 12. App Br. 14. Moreover, although Appellants separately argue for the patentability of claims 5, 6, 8, 10, 22–28, and 35, Appellants' arguments do not differ from the arguments Appellants make for the patentability of claim 1. Instead, for each these claims, Appellants argue that since "Lakhat does not disclose a pulse generator" as argued with respect to claim 1, Lakhat cannot disclose a pulse generator having the various properties or functionality further recited in claims 5, 6, 8, 10, 22–28, and 35. App Br. 15, 17, 19, 21, 24–27, 29, 31–36, and 52–53.

Consequently, we sustain the Examiner's rejection of claims 2–12, 22–28, and 35 for the same reason we sustain the Examiner's rejection of claim 1.

II. Whether Lakhat's command register is directly coupled to two processors recited in claim 29.

Claim 29 recites the system of claim 22, "wherein the at least one pulse generator is a single pulse generator directly connected to the at least two processors." Claims App'x. The Examiner finds Lakhat's Figures 2 and 3, which show register 50 connected to processor 14 and register 60 connected to processor 32, teach or suggest a single pulse generator connected to at least two processors. Ans. 14. Appellants argue the Examiner has erred because the Examiner has failed to consider the language of claim 29, and in particular because:

> [N]either of the registers 50 and 60 is directly connected to both of the processors 14 and 32. At most, each of the registers 50 and 60 is directly connected to only one of the processors 14 and 32. For example, the register 50 is connected to the processor 32 through a bus 30 and the register 60, which is not a direct connection.

App. Br. 39. We find Appellants' argument persuasive.

In rejecting claim 1, the Examiner found Lakhat teaches register 94 (a subcomponent of register 60) is a pulse generator. However, as Appellants argue, although Lakhat discloses register 60 is directly connected to processor 32, Lakhat fails to disclose register 60 is also directly connected to processor 14. Lakhat Figs. 2–3. Rather, Lakhat discloses register 60 is indirectly connected to processor 14 through registers 50/74. *Id*. Consequently, we do not sustain the Examiner's rejection of claim 29.

The Examiner rejected claims 37, 41, and 43, which recite similar features related to registers connected directly to a processor, on the same grounds as the rejection of claim 29. Ans. 14, and 16–18. For the same reasons stated for claim 29, we do not sustain the Examiner's rejection of claims 37, 41, and 43.

III. Whether the Examiner has established a prima facie case for the obviousness of claim 30.

The Examiner finds "[t]he limitations of claim 30 are rejected in the analysis of claim 22, and the claim is rejected on that basis." Ans. 14. Appellants argue the Examiner has failed to establish a prima facie case of obviousness because "claim 30 recites features that are not recited in claim 22 (e.g., at least one pulse generator connected to an interrupt control of peer processors)." App. Br. 40–41. In addition, Appellants argue claim 30 is patentable because "Lakhat does not disclose a pulse generator," and therefore cannot disclose a pulse generator having the functionality further recited in claim 30. App. Br. 42.

We find Appellants' argument unpersuasive. We addressed Appellants' pulse generator argument with respect to the Examiner's rejection of claim 1, and found it unpersuasive for the reasons noted *supra*. Nor are we persuaded by Appellants' argument the Examiner has failed to establish a prima facie case of obviousness by not specifically addressing the interrupt control limitation recited in claim 30.

"[T]he prima facie case is merely a procedural device that enables an appropriate shift of the burden of production." *Hyatt v. Dudas*, 492 F.3d 1365, 1369 (Fed. Cir. 2007). It is established when the Examiner

"adequately explain[s] the shortcomings [the Examiner] perceives so that the applicant is properly notified and able to respond" to the rejection. *Id.* at 1370. Contrary to Appellants' contention, "[t]here has never been a requirement for an examiner to make an on-the-record claim construction of every term in every rejected claim and to explain every possible difference between the prior art and the claimed invention in order to make out a prima facie rejection." *In re Jung*, 637 F.3d 1356, 1363 (Fed. Cir. 2011).

In the instant case, the Examiner rejected claim 30, which contains nearly identical language to claim 22, on the same basis as claim 22. In rejecting claim 22, the Examiner found Lakhat discloses two processors (RP processor 14 and NMP processor 32) and a pulse generator (command register 50) connected to a bus 30. Ans. 11–12 (citing Lakhat 3:44–47, Figs. 1–3). The Examiner relied on the same disclosure to reject claim 1, which recites a pulse generator directly connected to a processor's *interrupt control*. Ans. 6; Claims App'x. Figure 3 of Lakhat shows RP command register 50 connected to the interrupt control of RP processor 14 via RP IPC control and status register 82, and connected to the interrupt control of NMP processor 32 via IPC bus 30 and NMP IPC control and status register 102 of NMP command register 60. In view of these disclosures, we find the Examiner has established a prima facie case that the subject matter recited in claim 30 is obvious, and sustain the Examiner's rejection. *See Hyatt v. Dudas*, 492 F.3d at 1370.

Appellants do not argue for the patentability of claim 34 separately from the patentability of claim 30. App. Br. 43. Moreover, while Appellants separately argue for the patentability of claims 31–33, Appellants' arguments do not differ from the arguments Appellants make for

the patentability of claims 22 and 30. App. Br. 44, 46, 49. Consequently, we sustain the Examiner's rejection of claims 31–34 for the same reason we stated for claim 30.

IV. Whether Lakhat's command register and processors are directly connected to a bus-arbiter or switch recited in claim 36.

Claim 36 recites the method of claim 1, "wherein the first processor, the at least one pulse generator, and the at least a second processor are directly connected to one of an on-chip bus arbiter and an on-chip crossbar/switch." Claims App'x. The Examiner finds Lakhat's disclosure of IPC bus 30 in Figures 1–3 teaches or suggests a first processor, a second processor, and a pulse generator directly connected to an on-chip bus arbiter or crossbar/switch. Ans. 16 (citing Lakhat Figs. 1–3). Appellants argue the Examiner has erred because:

> [T]he RP processor 14, the RP IPC Comm Reg 50 (or the NMP IPC Comm Reg 60), and the NMP processor 32 are not directly connected to a same bus, *e.g.*, the first processor bus 15, the second processor bus 15, or the IPC bus 30. At most, the RP processor 14 and RP IPC Comm Reg 50 are connected to the first processor bus 15, the RP IPC Comm Reg 50 and the NMP IPC Comm Reg 60 are connected to the IPC bus 30, and the NMP processor 32 and the NMP IPC Comm Reg 60 are connected to the second processor bus 15. That is, both the RP processor 14 and the NMP processor 32 are not directly connected to either the first processor bus 15 or the second processor bus 15, and contrary to the Examiner's assertions, neither the RP processor 14 nor the NMP processor 32 are directly connected to the IPC bus 30. There is also no indication in Lakhat that the first processor bus 15, the IPC bus 30, and the second processor bus 15 are the same bus.

App. Br. 55. We find Appellants' argument persuasive.

In rejecting claim 1, the Examiner found Lakhat teaches or suggests a first processor (RP processor 14), a second processor (NMP processor 32) and a pulse generator (command register 94). Ans. 6 (citing Lakhat 3:44–47). However, as Appellants assert, Lakhat fails to teach or suggest RP processor 14 or NMP processor 32 are directly connected to IPC bus 30. Lakhat Figs. 1–3. Rather, Lakhat teaches RP processor 14 is indirectly connected to IPC bus 30 via RP system controller 18, and NMP processor 32 is indirectly connected to IPC bus 30 via NMP system controller 34. *Id*. Consequently, we do not sustain the Examiner's rejection of claim 36.

The Examiner rejected claims 38, 40, and 42 which recite similar features related to the pulse generator connected directly to one of an on-chip bus arbiter and an on-chip crossbar/switch, on the same grounds as the rejection of claim 36. Ans. 16–18. For the same reasons stated for claim 36, we do not sustain the Examiner's rejection of claims 38, 40, and 42, as well as claim 39 dependent therefrom.

V. Whether a computer usable storage medium includes transitory signals and signal propagation media recited in claim 35.

The Examiner rejected claim 35 as directed to unpatentable subject matter, finding the "computer usable storage medium" recited in claim 35 included signal transmission media. Ans. 5. Appellants argue the term "storage medium" is defined in the Specification, and "the claimed term 'storage medium' cannot be reasonable interpreted to cover transitory propagating signals *per se* in view of Appellants' specification." App. Br. 6 (citing Spec. 18:13–16, 22:1–14). Appellants further reply the Board has found claims directed to "computer readable storage medium" to be directed

to patentable subject matter. Reply Br. 3. We are not persuaded by Appellants' arguments.

First, the *Ex parte Hu*[5] decision cited by Appellants for the proposition that claims to computer readable storage media are statutory is non-precedential, and not binding on the Board. By contrast, the subsequently issued decision in *Ex parte Mewherter* addressing the same issue is a precedential decision that is binding on the Board. *See Ex parte Mewherter*, 107 USPQ2d 1857 (PTAB 2013). In *Mewherter*, the Board determined, absent an express limitation in the specification, "the ordinary and customary meaning of 'computer readable storage medium' to a person of ordinary skill in the art was broad enough to encompass both non-transitory and transitory media." *Mewherter*, 107 USPQ2d at 1860. Consequently, the Board found "the claim term 'machine-readable storage medium' would include signals *per se*. . . . [and] must be rejected under 35 U.S.C. § 101 as covering non-statutory subject matter." *Id.* at 1862.

Second, neither portion of the Specification identified by Appellants defines a "computer usable storage medium," or expressly limits its meaning to the statutory, non-transitory storage medium. Rather, the first portion simply provides an enumerated list identifying different types of storage media, "such as a diskette, hard disk, CD-ROM, DVD-ROM or tape." Spec. 18:13–16. While all the storage media identified in the list happen to be non-transitory, the list itself is open-ended and therefore does not limit storage media to non-transitory media. Similarly, the second portion provides an open-ended list of computer-usable or computer readable media, which "can be any apparatus that can contain, store, communicate,

[5] *Ex parte Hu*, 2012 WL 439708 (BPAI Feb. 9, 2012).

propagate, or transport [a] program for use by or in connection with [an] instruction execution system, apparatus, or device." Spec. 22:4–7. The computer usable or readable "medium can be . . . a propagation medium." *Id*. at 22:8–10.

In view of these disclosures, the Examiner finds the computer readable storage medium recited in claim 35 "can be reasonable [sic] interpreted to include the medium defined on page 22 of the current specification that includes signals." Ans. 20. We agree, and sustain the Examiner's rejection of claim 35 as directed to non-statutory subject matter. *Mewherter*, 107 USPQ2d at 1860.[6]

DECISION

For the reasons indicated above, we affirm Examiner's rejection of claims 1–12, 22–28, and 30–35, and reverse the Examiner's rejection of claims 29, and 36–43.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv) .

AFFIRMED-IN-PART

msc

[6] We note the Office has indicated Appellants may overcome this rejection by amending claim 1 to include the limitation "non-transitory." *See* David J. Kappos, *Subject Matter Eligibility of Computer Readable Media*, 1351 Off. Gaz. Pat. Office 212 (Feb. 23, 2010).