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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte SEHAT SUTARDJA, PANTAS SUTARDJA, and WILLIAM LO

Appeal 2010-004119
Application 11/196,651
Technology Center 2100

Before DENISE M. POTHIER, ANDREW CALDWELL, and JENNIFER S. BISK, *Administrative Patent Judges*.

POTHIER, *Administrative Patent Judge.*

DECISION ON APPEAL

STATEMENT OF THE CASE

Appellants appeal under 35 U.S.C. § 134(a) from the Examiner's rejection of claims 11-20 and 25-29. Claims 1-10 and 21-24 have been canceled. App. Br. 5.[1] We have jurisdiction under 35 U.S.C. § 6(b). We affirm.

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[1] Throughout this opinion, we refer to (1) the Non-Final Rejection mailed August 15, 2008; (2) the Appeal Brief filed August 28, 2009; (3) the Examiner's Answer mailed October 27, 2009; and (4) the Reply Brief filed December 21, 2009.

Invention

Appellants' invention relates to a self-reparable semiconductor with functional units that perform the same function. *See generally* Spec. ¶ 0002. Claim 11 is reproduced below with a certain limitation emphasized:

> 11. A self-reparable semiconductor including a graphics processing unit (GPU), comprising:
>
> *M pixel processors that perform a first function*, where M > 1;
>
> at least one spare pixel processor that performs said first function and that is functionally interchangeable with said M pixel processors; and
>
> switching devices that communicate with said M pixel processors and said at least one spare pixel processor and that can selectively replace any of said M pixel processors with said spare pixel processor when said one of said M pixel processors is inoperable.

The Examiner relies on the following as evidence of unpatentability:

Gordon	US 4,882,687	Nov. 21, 1989
Eckhoff	US 5,896,370	Apr. 20, 1999
Adamovits	US 6,618,819 B1	Sept. 9, 2003

The Rejections

1. The Examiner rejected claims 11-16, 18, and 25-29 under 35 U.S.C. § 103(a) as unpatentable over Adamovits and Gordon. Ans. 3-8.

2. The Examiner rejected claims 17, 19, and 20 under 35 U.S.C. § 103(a) as unpatentable over Adamovits, Gordon, and Eckhoff. Ans. 8-9.

THE OBVIOUSNESS REJECTION OVER ADAMOVITS AND GORDON

The Examiner finds Adamovits discloses all the limitations in representative claim 11, except for the processors being pixel processors. Ans. 3-4. The Examiner relies on Gordon to cure this feature and provides a

reason to combine Gordon with Adamovits. Ans. 4 (referring to claim 1), 10-12; *see also* Non-Final Rej. 3.[2]

Appellants argue that Gordon teaches only a single pixel processor and thus combining Gordon's teaching with Adamovits would only result in a single pixel processor in Adamovits' device performing a first function. App. Br. 9-10. Appellants further contend that the Examiner has failed to provide a reason for combining Gordon's pixel processor with Adamovits' telecommunication system. App. Br. 10-12.

ISSUES

(1) Under § 103, has the Examiner erred in rejecting claim 11 by finding that Adamovits and Gordon collectively would have taught or suggested M pixel processors performing a first function?

(2) Is the Examiner's reason to combine the teachings of these references supported by articulated reasoning with some rational underpinning to justify the Examiner's obviousness conclusion?

[2] MPEP § 1207.02 states, "[a]n examiner's answer should *not* refer, either directly or indirectly, to any prior Office action without fully restating the point relied on in the answer" (emphasis added). Yet, both the Examiner's Answer and the Final Rejection mailed January 28, 2009, refer to canceled claim 1 for the motivational statement, which is discussed in the Non-Final Rejection mailed August 15, 2008. Since Appellants discuss the findings found in the Non-Final Rejection (*see* App. Br. 10 (quoting the Examiner's reasoning provided in the Non-Final Rejection)), we likewise will refer to this Non-Final Rejection throughout the Opinion.

ANALYSIS

Based on the record before us, we find no error in the Examiner's rejection of claim 1 which calls for a device having M pixel processors that perform a first function. The Examiner finds that Adamovits discloses M processors that perform a first function (e.g., loading software into the processors and commencing loaded software routines) and spare processors for these M processors. *See* Ans. 3, 10-11 (citing col. 2, ll. 25-33; col. 3, ll. 56-65; Fig. 7). Notably, these findings have not been challenged by Appellants (*see* App. Br. 9-12), and thus the record contains undisputed findings that Adamovits teaches M processors that perform a first function.

Appellants instead argue that that Adamovits fails to teach M *pixel* processors. App. Br. 9. The Examiner admits as much, when stating that Adamovits "does not teach the processor being a pixel processor." Ans. 4. The Examiner turns to Gordon for such a teaching and suggests modifying Adamovits sparing system with Gordon pixel processor. *See* Ans. 4, 10-11; *see also* Non-Final Rej. 4. Appellants argue that Gordon only teaches a single pixel processor and thus any modification of Adamovits based on Gordon would not result in multiple pixel processors. App. Br. 10-12. We disagree.

While perhaps not described in the clearest manner, the Examiner's proposed rejection does not suggest only modifying one processor in Adamovits for a pixel processor as a taught by Gordon. The Examiner proposes "combin[ing] the sparing system for n pieces of equipments of Adamovits with Gordon pixel processor for the sparing of *pixel* processor*s* in a critical system." Ans. 11 (emphases added). Additionally, the Examiner finds that Adamovits teaches using one sparing piece of

equipment for each n pieces of equipment in the system, suggesting that this spare equipment substitutes for each n pieces of equipment. *See* Ans. 12. The import of these statements made by the Examiner signifies that the combination would substitute each of Adamovits sparing processors (e.g., Fig. 7, 106a-b) with a pixel processor as taught by Gordon, predictably yielding multiple spare pixel processors. Thus, looking at the rejection as whole, combining Gordon with Adamovits, as proposed, also suggests substituting Adamovits' multiple processors with multiple pixel processors such that the substituted spare pixel processors are spare processors for M processors discussed in Adamovits. We therefore find that the proposed combination teaches and suggests M pixel processors that perform a first function as recited in claim 11.

Appellants further assert that the Examiner fails to provide an explicit reason for combining Gordon with Adamovits and that an ordinarily skilled artisan would not have combined Adamovits telecommunication system with Gordon's pixel processor. App. Br. 10-12. We first note that an obviousness analysis need not include a precise teaching but must have "some articulated reasoning with some rational underpinning to support the legal conclusion obviousness." *See KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007) (citation omitted). The Examiner explains (Ans. 11-12 (citing col. 3, ll. 45-54)) that while Adamovits discusses critical telecommunication and data systems using spare processors, Adamovits further contemplates that such a system has "wide applicability to sparing for critical equipment in a wide variety of applications and environments." Col. 3, ll. 53-54.

Thus, Gordon was cited as an example of a known processor environment (e.g., a pixel processing environment) where Adamovits' wide applicability for sparing critical equipment can be used to ensure acceptable operations specifically for pixel processors. *See* Ans. 11-12; *see also* Non-Final Rej. 3. Once again, while not stated in the clearest way, we agree with the Examiner and find that an ordinarily skilled artisan would have recognized that a critical system like Adamovits's Figure 7 having redundancies for processors would have lend itself to various environments, including those having pixel processors taught by Gordon. *See* Ans. 11-12; *see also* Non-Final Rej. 3. That is, employing the inferences and creative steps that an ordinarily skilled artisan would have used, we find that ordinarily skilled artisan would have recognized the benefits of applying such a redundant system to a multiple pixel processor environment. *See KSR*, 550 U.S. at 418.

Appellants do not address or counter in the Reply Brief the Examiner's articulated reasons for combining Adamovits and Gordon discussed in the Response to Arguments section, but rather repeat that Adamovits discusses a telecommunication switch and Gordon discusses a single pixel processor. *See* Reply Br. 8-9. Also, notably, the Examiner's finding (Ans. 3) that Adamovits is a self-reparable semiconductor having a GPU has not been disputed. *See* App. Br. 9-12. We therefore find that the Examiner has provided some articulated reasoning with some rational underpinning to support a legal conclusion of obviousness. *See KSR*, 550 U.S. at 418.

For the foregoing reasons, Appellants have not persuaded us of error in the rejection of independent claim 11 and claims 12-16, 18, and 25-29 not separately argued with particularity (App. Br. 12).

THE REMAINING REJECTION

The Examiner finds that Adamovits, Gordon, and Eckhoff teach all the limitations in claims 17, 19, and 20. Ans. 8-9. For this rejection, Appellants refer to the previous arguments made for claims 11 and 25. App. Br. 13. The issues before us, then, are the same as those in connection with claims 11 and 25, and we refer to our previous discussion. We need not address whether Eckhoff cures any purported deficiency in Adamovits or Gordon. App. Br. 13.

CONCLUSION

The Examiner did not err in rejecting claims 11-20 and 25-29 under § 103.

DECISION

The Examiner's decision rejecting claims 11-20 and 25-29 is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED

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