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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Inter Partes

RAMBUS, INC.
Patent Owner, Appellant

v.

NVIDIA, CORP.
Requester (Withdrawn)

Appeal 2013-000562
Reexamination Control No. 95/001,169
United States Patent 6,591,353 B1
Technology Center 3900

Before ALLEN R. MacDONALD, KARL D. EASTHOM, and STEPHEN C. SIU, *Administrative Patent Judges*.

EASTHOM, *Administrative Patent Judge*.

DECISION ON APPEAL

This reexamination proceeding (95/001,169) returns to the Board after the *Examiner's Determination Under 37 C.F.R. 41.77(d)* (April 19, 2012) which responds to the Board's rejections designated as new grounds in its previous *Decision on Appeal, Inter Partes NVIDIA, Corp. v. Rambus, Inc.*, BPAI 2011-010623 (Jan. 24, 2012) involving Patent Owner Rambus's '353 patent at issue here.[1] We have jurisdiction under 35 U.S.C. §§ 134(b) and 306.

The previous Board Decision, BPAI 2011-010623, is sustained and is part of this decision.

STATEMENT OF THE CASE

In the above-described '623 Board Decision, the Board, in a bifurcated decision, affirmed the Examiner's decision to maintain the rejection of claims 1, 5, 7, 11, 14, 19, and 23 cross-appealed by Rambus, and reversed the Examiner's decision not to reject claims 1-26 appealed by Third-Party Requester NVIDIA. (*See* '623 Bd. Dec. 45.) As to the reversal, pursuant to 37 C.F.R. § 41.77(b), the '623 Board Decision reversed the portion of the Examiner's Answer (which incorporates by reference the Examiner's Right of Appeal Notice) in which the Examiner decided not to maintain NVIDIA's proposed rejections, and the Board designated the reversal "a new ground of rejection." (*See* '623 Bd. Dec. 45 n. 12.)[2]

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[1] U.S. 6,591,353 B1 to Barth et al., *Protocol For Communication with Dynamic Memory* (July 8, 22, 2003).

[2] The rejections are designated as "new ground[s]" under 37 CFR § 41.77(b) because the Examiner decided not to adopt or maintain them and the Board reversed the Examiner. Notwithstanding the "new ground" designation,

In response to the '623 Board Decision, Rambus elected the 37 C.F.R. § 41.77(b) (1) option of reopening prosecution before the Examiner to address the new grounds of rejections (originally proposed by NVIDA, *see* note 2 *supra*) and presented new evidence to rebut the "new ground[s] of rejection" by the Board as required under 37 C.F.R. § 41.77 (b) (1) & (d). (*See* Rambus's *Request to Reopen Prosecution* (Feb. 24, 2012).) Prior to Rambus's *Request to Reopen* and after the '623 Board Decision, NVIDIA, citing a settlement with Rambus, withdrew from the reexamination proceeding. (*See Notice of Withdrawal of Third-Party Requester's Appeal and Other Papers* (Feb. 17, 2012); *Notice of Non-Participation in Inter Partes Reexamination* (Feb. 8, 2012).)

Under 37 C.F.R. § 41.77(d), the prior '623 Board Decision is "binding upon the examiner unless an amendment or new evidence not previously of record is made which, in the opinion of the examiner, overcomes the new ground of rejection stated in the [Board's '623] decision." Further pursuant to 37 C.F.R. § 41.77(d), the Examiner must consider Rambus's *Request to Reopen* and "issue a determination that the rejection is maintained or has been overcome."

Pursuant to 37 C.F.R. § 41.77(d), the Examiner determined that Rambus's *Request to Reopen* did not overcome the "new ground[s]" of rejections. In the Examiner's *Determination*, the Examiner considered Rambus's newly submitted evidence as discussed further below (which

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third-party Requester NVIDIA originally proposed the rejections in its *inter partes* request, though some grounds thereof ultimately were remanded with modification to the rationale and/or findings. (*See* Bd. Dec. 26-27 (listing NVIDIA's originally proposed rejections).)

includes a Third Supplemental Declaration by Rambus's expert Robert J. Murphy and other extrinsic evidence including publications by one of NVIDIA's experts). (*See* Reopen Req. 2.)

The following "new ground[s] of rejection" listed in the '623 Board Decision are addressed in the Examiner's *Determination* and are at issue here:

Claims 2, 6, 10, 17, 25, and 26 as obvious under 35 U.S.C. § 103(a) based on Hayes and Bennett et al., U.S. Patent 4,734,909 (Mar. 29, 1988) ("Bennett").

Claims 3, 4, 12, 13, 21, and 22 as obvious under 35 U.S.C. § 103(a) based on Hayes, Bennett and Inagaki, JP 57-210495 (Dec. 24, 1982).

Claims 12 and 13 as obvious under 35 U.S.C. § 103(a) based on Hayes and Inagaki.

Claims 2-10, 12-14, 16, 17, and 20-26 as obvious under 35 U.S.C. § 103(a) based on Hayes and Ohshima et al., *High Speed DRAMs with Innovative Architectures* IEICE Trans. Electron V. ECC-7, No. 8, 1303-15 (Aug. 1994) ("Ohshima").

Claims 1-14, 16, 17, and 19-26 as obvious under 35 U.S.C. § 103(a) based on Kushiyama, Hayes, and Lu, *The Future of DRAMs*, 1988 IEEE Inter. Solid-State Cir. Conf. (ISSCC), Digest Tech. Papers, 98-99 (Feb. 1988)("Lu").

Claims 1-4, 6-9, 11-13, 15, 16, 18-22, and 24-26 as obvious under 35 U.S.C. § 103(a) based on Farmwald et al., U.S. 5,319,755 (June 7, 1994) ("Farmwald '755") and Lu.

Claims 1-4, 6-9, 11-13, 15, 16, 18-22, and 24-26 as obvious under 35 U.S.C. § 103(a) based on Farmwald '755 and iRAM, *Memory Components Handbook*, Intel. Corp., Ch. 1, 3 (1985).

(*See* '623 Bd. Dec. 27.)

Exemplary claims of the '353 patent under reexamination follow:

1. A method of operation in a memory device that includes a plurality of memory cells, the method comprising:
receiving a command to sample data;
deferring sampling a first portion of the data until an external strobe signal is detected; and
sampling the first portion of the data from an external signal line in response to detecting the external strobe signal.

2. The method of claim 1, wherein the first portion of the data is sampled synchronously with respect to an external clock signal.

5. The method of claim 1, further comprising:
detecting an external terminate signal; and
sampling additional portions of the data during a time interval between detection of the external strobe signal and detection of the external terminate signal.

11. A method of controlling a memory device that includes a plurality of memory cells, the method comprising:
issuing a first write command to the memory device, the memory device being configured to defer sampling data that corresponds to the first write command until a strobe signal is detected;
delaying for a first time period after issuing the write command; and
after delaying for the first time period, issuing the strobe signal to the memory device to initiate sampling of a first portion of the data by the memory device.

19. A memory device having a plurality of memory cells, the memory device comprising:

a plurality of input receiver circuits to receive a write command and sample data that corresponds to the write command in response to detecting a strobe signal that is delayed relative to the write command by a first time period.

DICUSSION

Pursuant to 37 CFR § 41.77(f) and the new grounds of rejection issued in the '623 Board Decision, the Board hereby "reconsiders the matter and issue[s] a new decision. The new decision . . . incorporate[s] the earlier ['623Board D]ecision, except for those portions specifically withdrawn." No such portions are withdrawn.

The Examiner's Determination is also hereby adopted and incorporated by reference. Rambus did not file "comments in response to the [E]xaminer's [D]etermination" as allowed under 37 CFR § 41.77(e) to rebut or show error in the Examiner's Determination with respect to the new grounds.

Preliminary Remarks – Bifurcated Proceeding

Aside from the new grounds of rejection, as the Examiner reasons, Rambus improperly also seeks review *before the Examiner* in the bifurcated portion of the requested review which involves the Examiner's anticipation rejection of claims 1, 5, 7, 11, 14, 19, and 23 based on Hayes which Rambus cross-appealed and which the Board affirmed in the '623 Board Decision. (*See* Ex. Det. 4-5; Reopen Req. 3-14; Bd. Dec. 7-16.) Reopening prosecution under 37 CFR § 41.77(b) is only "one of the . . . two [possible] options . . . *with respect to the new ground of rejection*." *Id*. (emphasis added). The affirmed rejection was not part of any "new ground of

rejection" under the rule and the Examiner properly refused to consider Rambus's request for review of the affirmed rejection. (*See* Ex. Det. 4-5.)

Subsequent to the underlying '623 Board Decision, the Board began issuing clarifying information for situations such as this which involve new grounds of rejection. (*See, e.g*., PTAB 2012-001976 at 43-45 (clarifying information related to new grounds).) Under the circumstances involved here, the portion of Rambus's Response with respect to the affirmed rejection appealed by Rambus is not responsive to the new grounds but is deemed to be in the nature of a request for rehearing under 37 CFR § 47 (Rehearing).

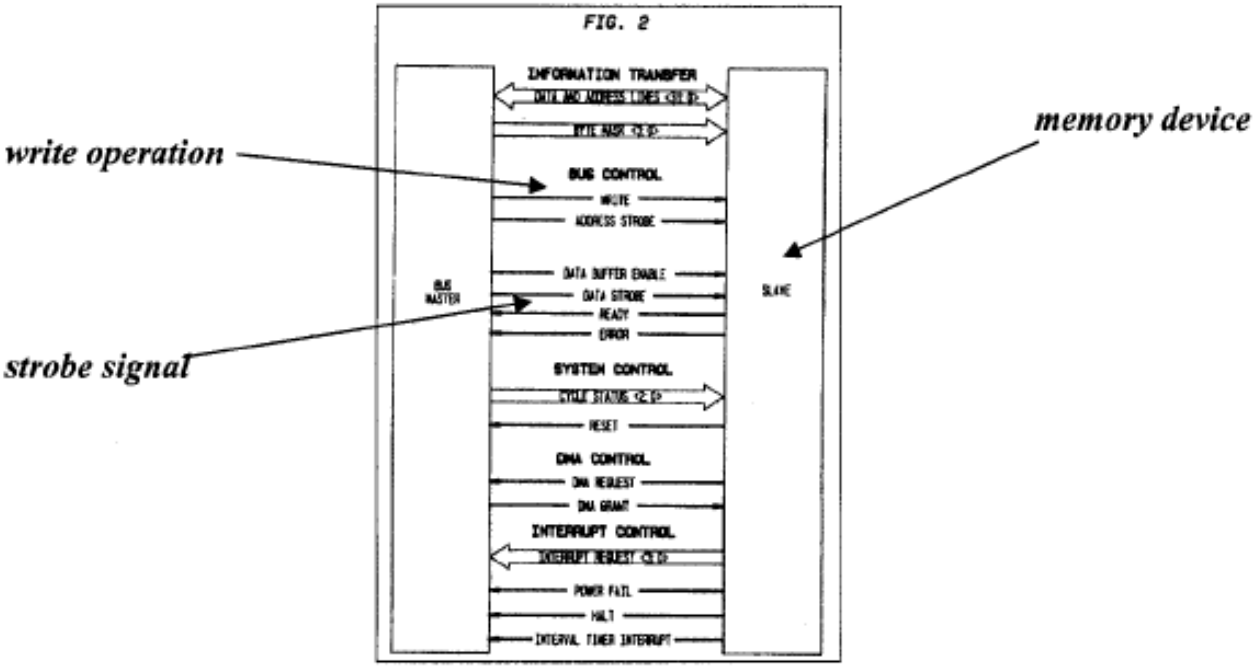
With further respect to the affirmed rejection based on anticipation by Hayes, a primary point of contention involves the "strobe signal" element recited in the independent claims. The "strobe signal" is also an element in the dependent claims which are involved in the new grounds of rejection based on obviousness over Hayes. Accordingly, some substantive issues overlap between the two portions of the bifurcated proceeding. As such, the Board exercises its discretion and addresses all of Rambus's arguments and new evidence to expedite the proceeding with special dispatch as 35 U.S.C. § 314 (c) mandates, to avoid further unnecessary procedural issues, to afford Rambus a fair hearing, and to provide a record summary.

Hayes –Anticipation - Rehearing

NVIDIA argued, and the Examiner and the Board found, that the Hayes memory device as represented in the figure below anticipates claims 1, 5, 7, 11, 14, 19 and 23 of the '353 patent. (*See* '623 Bd. Dec.5-26.) Rambus's arguments focus on claim 1 which is hereby selected to be representative of claims 1, 7, 11, and 19. For the most part, notwithstanding

the new evidence proffered, the arguments restate or repackage similar arguments made in the original appeal without adding sufficient or probative evidence which shows that the '623 Board Decision overlooks or misapprehends the teachings of Hayes as applied to the claims at issue.

Hayes's Figure 2, as annotated by NVIDIA, appears next:



Hayes, Fig. 2

Annotated Figure 2 shows Hayes's slave memory device. (*See* NVIDA App. Br. 7 (addressed further in the underlying '623 Board Decision).)

Rambus argues, relying on its expert declarant Murphy, that the Hayes "Data Strobe" (*see* Fig. 2 above) ("DS") signal is not an external strobe signal as recited in claim 1. (*See* Reopen Req. 6-8 (citing Murphy 3rd Supp. Decl. ¶¶ 5-9).) The '623 Board Decision addresses this repackaged argument: "Claim 1 'defer[s] sampling . . . until an external strobe signal is

detected' and does not require an immediate response to the strobe signal." ('623 Bd. Dec. 22.) The '623 Board Decision explains that the DS signal, a "data strobe" signal, constitutes a strobe signal which "tells the slave memory device in Hayes that the data is valid on the bus so that the slave memory device knows when to sample (read) it." ('623 Bd. Dec. 21.)[3]

Murphy's new testimony and Rambus's arguments do not rebut these facts or other facts or rationale in the '623 Board Decision with a necessary evidentiary underpinning. Similar to Rambus, as an example, Murphy testifies that "multiple signals . . . are asserted when sampling is alleged to occur in Hayes" and this shows that none of those signals "initiate sampling." (Murphy 3rd Supp. Decl. ¶ 8.)[4]

But nowhere does Murphy even assert, much less show, that the Hayes memory device does not defer sampling until the after the DS is detected as claim 1 requires. Murphy also does not show that the memory device does not sample data in response to the DS as called for in claim 1. As the '623 Board Decision finds, Hayes states that "'[d]uring a write cycle, the bus master asserts DS to indicate that DAL [31:0] contains valid write data. The bus master then deasserts DS to indicate that it is about to remove the write data from the DAL [31:0].'" ('623 Bd. Dec. 9 – listing fact H2 (i.e., quoting Hayes).) The Decision also relies on Hayes which states that

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[3] As used here, a *read by* the memory device in Hayes also constitutes a *write to* the device – in both cases, a "sample" by the memory device.

[4] Such arguments and new evidence technically are not proper in a request for rehearing since the Board could not have overlooked such evidence, but the evidence is similar to previous evidence submitted and addressed to expedite this bifurcated proceeding on the merits as indicated at the outset.

for a write cycle, "'[t]he bus master ... drives data onto DAL 31:0] and asserts DS [data strobe col. 7, 1. 56], indicating that the data is valid on DAL [31:0]. If no error occurs, the slave device reads the data.'" ('623 Bd. Dec. 9, H2 (quoting Hayes).)

The Decision also explains that claim 1 and the '353 patent disclosure include a delay after the DS (e.g., waiting until several cycles of an external clock signal) and do not preclude other subsequent control, and Rambus "corroborates" this understanding and "describes a similar delay between the data and the strobe." (*See* '623 Bd. Dec. 22 (citing P.O. Cr. App. Br. 10; Req. Resp. Br. 12).)

In response to the '623 Board Decision, Murphy also avers that other signals in Hayes enable the data transceivers 57 and that the RAM control logic 62 receives the DS signals but the "'memory devices' represented by the 256Kbit DRAM chips 64" do not receive the DS signal. (*See* Murphy 3rd S. Decl. ¶¶ 9-10.) The Board accepts that testimony as it appears to be supported by Hayes, but that testimony does not upset the '623 Board Decision. For example, as to the latter point, the '623 Board Decision does not rely on one DRAM chip as the recited memory device. Rather, as indicated in the annotated Figure 2 *supra*, the Board relies on the whole memory/slave board in Hayes which includes the RAM control logic 62 and which therefore receives the DS as claim 1 requires.

Murphy also explains that "RAM control logic 62 is not connected to any other device that receives data on DAL [31:0]" and also opines that the error signal which might occur after the DS in Hayes shows that DS does not satisfy the strobe signal recited in the claims. (*See* Murphy 3rd S. Decl. ¶ 9-

10.) Rambus makes similar arguments, relying on Murphy. (*See* Reopen Req. 6-10.)

The Board was cognizant of how the Hayes system operates based on related arguments and findings, including details about the error signal and the transceivers. As Rambus's expert Murphy points out, the transceivers become enabled during the data transfer process, but this simply agrees with the Board's finding that the external data lines DAL[31 :0] and DATA <31 :0> lines on the memory board become connected directly together through the enabled transceivers 57 on the memory board in Figure 7. (*See* '623 Bd. Dec. 24, n. 6 (citing Parris Declaration).) As NVIDIA's expert Parris testifies, "[t]owards the end of a write cycle, when data is being transmitted to the slave device, the DATA TRANSCEIVER 57 connects DAL[31 :0] directly to DATA <31 :0>." (Parris Decl. 15.) Murphy's new testimony and Parris's testimony coalesce on that point.

Rambus's assertion that "the RAM control logic 62, which receives the DS signal, is not connected to the data and address and [control] lines DAL[31 :0] or even to the device [transceiver 57] that is connected to DAL[31 :0]" (*see* Reopen Req. 9), is not material given the finding that the data lines external to and on the bus are connected via the transceiver prior to a data transfer. The enabled transceiver 57 directly connects the DRAM chips to the external DAL[31 :0], and therefore, the DS signal does "necessarily indicate[] whether valid data is on the separate data lines<31:00>," contrary to Rambus's argument (*see id*.), because the same data is on both connected lines - according to the un-rebutted findings based on the Parris, Murphy, and Hayes, and as outlined in in the '623 Decision as mentioned *supra*.

In other words, the DRAM chips sample the same data from DAL[31 :0] and data lines<31:00> through the enabled transceivers 57. The assertion of DS at the RAM control logic 62 input 62 which controls the DRAM chips initiates sampling by the DRAM chips of the data lines DAL[31 :0] and connected data lines<31:00>. Rambus's arguments and evidence do not rebut or even address with particularity the Board's summary finding: "In sum, the bus master asserts DS when data is valid on the bus, the slave *then* reads the data (absent an abnormal abort as discussed below), and then the bus master deasserts DS when data is about to be removed from the bus. (H2.)" ('623 Bd. Dec. 20 (emphasis added, citing "H2" facts found from Hayes).)

Rambus also does not rebut the underlying related finding that the slave memory device 15 responds to DS as the one-way DS (DATA STROBE) signal in Figure 2 shows, and as the noted passages show, the slave memory device reads the data after the DS in normal circumstances (i.e., when no abnormal error signal aborts the process as the '623 Board Decision explains). Rambus also does not point to any normal external signal to the memory device which occurs after the DS control signal and before sampling in Hayes.

Rambus's arguments reduce to its following statement by Rambus: "Merely because DS happens to be asserted when valid data is present and the alleged sampling in Hayes also happens to occur when valid data is present does not mean that DS causes the alleged sampling." (Reopen Req. 7.) To the contrary, without the DS which occurs before the sampling, sampling would not occur – as indicated, Rambus does not challenge the Board's finding that "'the bus master asserts DS when data is valid on the

bus, the slave *then* reads the data.'" (*See* Reopen Req. 7 (quoting '623 Bd. Dec. at 20, emphasis here).) As such, the Board shows a causal relationship, contrary to Rambus's argument that the Board "confuses coincidence with causation." (Reopen Req. 7; *accord* Parris Decl. ¶ 11 (discussing an analogous or similar TrncvrRW signal and explaining why indicating valid data to a slave indicates when to sample the data).)

Rambus also states that the memory device excludes an external bus controller. (*See* Reopen Req. 10-11.) But as Rambus also notes, the disclosed memory device is a slave device and has "some internal 'control logic.'" (*Id*. at 11 (citing Figs. 6 and 20 of the '353 patent).) Similarly, in Hayes, the memory controller 12 and other masters 10, 11 (Hayes Fig. 1) are external to the slave memory device 15, but the slave memory board includes some RAM "control logic" on the board. (*See* Hayes, Fig. 7.) In a related Rambus appeal, the Federal Circuit recently held that contrary to Rambus's similar arguments, the term "memory device" is not limited to a single chip and includes a memory board and some control logic.[5]

Rambus also asserts that the '353 patent specification exhibits an "explicit definition" which the Board overlooks. Rambus states that a "strobe signal" in the '353 patent means "'data transfer start information.'" (*See* Reopen Req. 8 (quoting '353 patent at col. 8, ll. 60-63).) The Board could not have overlooked this new evidence submitted by Rambus as part of this rehearing request.

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[5] *See In re Rambus Inc.*, 694 F.3d 42 (Fed. Cir. 2012) (holding that the claim term "memory device" in a related Rambus patent includes a memory board and is not limited to a single chip contrary to Rambus's similar arguments otherwise).

In any event, it is not clear how that disclosure distinguishes over Hayes. The Hayes DS includes "start information" by indicating valid data right before the data starts transferring. Moreover, the passage in the '353 patent relied upon by Rambus specifically describes "indicat[ing] when the DRAM is to begin *sending* data" (*id.* at ll. 63-64 (emphasis added)) but does not refer to when the DRAM begins *sampling* data. Rambus's Cross-Appeal Brief points to other passages which generically refer to transferring data in relation to the strobe signal, but the '623 Board Decision addresses variations of Rambus's argument and relies on NVIDIA's and Rambus's briefs which essentially agree that "the '353 patent describes a delay between the strobe signal and sampling" as noted *supra*. (*See* '623 Bd. Dec. at 22; P.O. Cr. App. Br. 10; Req. Resp. Br. 12.) Rambus fails to rebut these findings and explain how this limited disclosure of "start information" associated with the strobe signal and data transfers shows that the Board's interpretation of the Hayes DS signal which starts the sampling process is inconsistent with the '353 Patent Specification.

Also, Rambus does not explain clearly how the '353 patent "defines" a strobe signal or even when the DRAM begins *sending* data after the strobe signal, let alone when the DRAM *samples* data. According to the '353 patent, the DRAM begins to send data in what amounts to two different phases over several clock cycles after the strobe signal: the DRAM first accesses a column in the DRAM and then it sends the accessed data from the column onto an external bus. (*See* '353 patent, col. 21, ll. 13-21.) These unclear time distinctions for sending data upon which Rambus relies, and the seemingly related above-discussed time delays between the strobe signal and data transfer, do not define any clear distinction over Hayes which similarly

samples data in response to the DS signal. Moreover, though not required necessarily to support the Board's claim interpretation, these time delays between data transmission and the strobe signal as disclosed in the '353 patent indicate that something other than, or, in addition to, the disclosed strobe signal (i.e., perhaps stored or pre-programmed clock delay times) govern the actual timing of any data transmission after the data strobe.

Rambus's repackaged arguments that Hayes does not anticipate claims 5, 14, and 23 based on the recited "terminate signal" in those claims lack a citation to new evidence and also fail to show that the '623 Board Decision overlooks or misapprehends a material consideration. (*See* '623 Bd. Dec. 23-26; Reopen Req. 13-14.)

Based on the foregoing discussion, Rambus's new evidence and arguments fail to show that the '623 Board Decision overlooks or misapprehends a material consideration warranting a modification of the anticipation rejection of claims 1, 5, 7, 11, 14, 19, and 23 based on Hayes.

Remanded Proceeding

Hayes and Bennett – Claims 2, 6, 10, 17, 25, and 26

Rambus does not direct attention to a specific claim. Claim 2, taken to be representative, depends from claim 1 and further requires the "data [to be] sampled synchronously with respect to an external clock." On remand, "[t]he [E]xaminer does not find patent owner's evidence sufficient to overcome the Board's decision." (Ex. Det. 5.) The Examiner's findings and rationale are adopted and incorporated by reference and supported by the record.

As explained in the Decision and under *In re Rambus* (*supra* note 5), the Hayes memory device satisfies the claim 1 memory device. (*See* '623

Bd. Dec. 28-29.) The combination of Bennett and Hayes renders obvious claim 2 even if it requires a single chip memory device as discussed further below. Bennett teaches a memory device receiving data synchronously with an external clock from a master, and Hayes teaches sending signals from a bus master to a slave memory device as depicted *supra* in Figure 2.

Rambus contests the Board's and the Examiner's finding that Bennett discloses a synchronous single chip memory device and that the combination with Hayes would have been obvious. (*See* Reopen Req. 14-21.) The contentions are addressed below after a summary of Bennett's teachings.

Bennett's Teachings

B1. Bennett's "paramount object" is to provide communication between "very large scale integrated VLSI (circuit) elements" (col. 12, ll. 14-18) – i.e., "VLSIC chips" (col. 9, ll. 35-40). Bennett discloses combining Versatile Bus Interfaces (VBI) and VLSIC "*upon the same chip substrate as the VLSI User Device*" (col. 12, ll. 29-32 (emphasis added)) with such a user device including "*interfaces intended to be built with* a CPU, IOC or *Memory*, or similar User device for signal or data exchange" (col. 35, ll. 59-62 (emphasis added)). (*See also* col. 14, ll. 19-24 (describing "interface to the user devices (usually upon the same chip substrate)".)

Bennett's Figure 1 represents a single chip User Device, which includes memory, as noted *supra*: "Each Versatile Bus Interface Logics, for example Versatile Bus Interface Logics 102a, interfaces a User module, for example VLSI Circuit User Device 106a which is pictorially represented in shadow line within FIG. 1 *as existing on the same VLSIC chip substrate* as Versatile Bus Interface Logics 102a." (Col. 36, ll. 19-24 (emphasis added).)

Bennett's chips have up to 120 pins as a practical limit. (Col. 9, ll. 60-61.) Bennett also discloses different memory types as "Fast Memory" or "Large Memory" with the memory having address widths of 16, 24, or 32, and one fast memory embodiment having 37 pins (col. 92, ll. 15-56; Fig. 32). One large memory has at least 16 pins to access 2^{32} addresses by employing two 16-bit address words over successive clock cycles. (*See* col. 95, ll. 59-60; Fig. 36.)

B2. Figure 38 shows "memories device" 3802c and 3802d connected to a "Versatile Bus." (Col. 97, ll. 8-10.) In the next paragraph, Bennett refers to "VSLI chips hav[ing] access to all Versatile Bus lines and therefore, the Versatile Bus protocols." (*Id*. at ll. 20-22.)

Bennett elsewhere refers to "memory devices" including, but not limited to, a ROM: "Not all memory devices can perform all operations; for example, read only memory (ROM) cannot execute the write operations." (Col. 90, l. 66 to col. 91, l. 2.) Bennett then refers to "[s]ample memory operations . . . defined in the following paragraphs" (col. 91, ll. 4-5) and thereafter describes "relatively small fast memories, and . . . larger and relatively slower memories" (col. 92, ll. 13-14).

Bennett also refers to "VLSIC chip devices" (col. 90, ll. 38-41) and in the next section, Section "4.1, Sample Memory Operations," states that "[m]any, if not most, applications of VLSIC technology are likely to include memory devices." (Col. 90, ll. 42-44.) Bennett generally discusses these chip devices as employing the interconnection protocol standards outlined generally in Section 3 and more specifically discusses memory devices in Section 4, including embodiments or configurations involved in Figures 31-36. (*See id*. at ll. 36-41.) For example, as discussed in Section 4 of Bennett,

Figures 32 and 33 represent fast memory read or write operations, with Figures 32 and 33 respectively signifying "DATA" transmission on 16 and 8 pins. Other pins are used for arbitration and slave ID. (*See* col. 93, l.12 - col. 94, l. 56.)

Figures 25a-h, represent more generic slave device configurations as discussed in Section 3 of Bennett. (Col. 25, l. 57 to col. 26, l. 11; *see generally* columns 81-88). Bennett also refers to the Section 3 figures as representing chips: "Section 3 provided for the electrical connection of many chips on one bus . . . . Each chip recognizes the existence of the transactions . . . ." (Col. 90, ll. 27-30.)

B3. In addition to chips, Bennett also discusses memory cards in Section 2, "Description of the Prior Art" (*see* col. 5, l.52 *et seq*.), and states that "the functionality of VLSIC chips is often similar to that of cards today" but that "VLSIC technology promises much higher performance than that of cards," even though cards hold more memory and chips have higher development costs. (Col. 9, ll. 43-56.) In the next passage, Bennett discusses creating larger chips to accommodate a greater numbers of pins. (Col. 9, l. 66 to col. 10, l. 29.)

B4. Bennett describes a "third physical objective" – the VBI (versatile bus interface) "should occupy a reasonable VLSI circuit substrate area" using fast and efficient CMOS technology as the preferred embodiment. (Col. 13, ll.18-23.) Typically, only about 20 VLSIC devices will be interconnected. As a "first logical object," the VBI logics "should offer a fixed format, simply controlled, powerfully featured interface to the user devices (usually upon the same chip substrate)" yet with certain options for use. (Col. 14, ll. 20-30.)

Bennett contemplates simple devices with "as few as three pins" (Bennett, col. 12, l. 61), or "pass[ing] but a single bit of data from a single master device to a single slave device . . . [or more bits and devices]. The versatility is from the trivial to the profound." (Col. 15, ll. 26, 42-50.) Figure 32, a "sample fast memory," has "an address field arbitrarily sized at four bits." (Col. 93, ll. 12, 23.) Generally, large memories are slower than, and have more address pins, than fast memories. (Co. 94, ll. 26-33.) Bennett mentions that for large memories, "[a]ddress width may be configured to 16, 24, or 32 bits to match requirements." (Col. 94, ll. 35-36.) In another section, Bennett describes a fast memory which may have 16 bit words, and if so, "at a 40 nanosecond pace may either have to be very wide or very fast or both." (Col. 89, ll. 30-32.) "The technology is projected to drive signals form chip to chip in 20 to 40 nanoseconds with internal gate delays of 1 to 2 nanoseconds." (Col. 9, ll. 57-60.)

B5. Bennett discloses synchronous clocked communication between bused VLSIC chips over 16 data lines at 25MHz, and notes that synchronous communication is more efficient than asynchronous communication. (Col. 13, ll. 3-17; col. 66, l. 9 – col 67, l. 18; col. 101, ll. 50-54 ("all communication . . . is synchronously referenced"); col. 101, ll. 51-54.) Bennett also states that the clock signals "are normally synchronous." (Col. 274, l. 62.)

B6. As noted *supra*, Bennett contemplates simple systems having "a single slave memory." (Col. 57, l. 57.) Bennett explains that "the number of [device] locations strongly affects complexity." (Col. 8, ll. 30-31.) Bennett distinguishes between slaves and masters: slaves "only respond to

information on the interconnect," masters "control the interconnect"; thus, slaves are subordinate to masters. (Col. 8, ll. 30-41.)

Analysis

Rambus's arguments do not focus on any particular claim. Claim 2 is selected to be representative. The '623 Decision reasons as follows:

> As NVIDIA persuasively explains, Hayes describes time-multiplexed clock data transfers between a master and slave during different clock cycles [*see* Hayes col. 19, ll. 45-46], and Bennett teaches benefits to providing a synchronized interface in a memory device using an external clock. (*See* Req. App. Br. 6-9; H6.)

('623 Bd. Dec. 29; *see also id*. at 6 – facts found in Hayes designated as "H6".)

Rambus's new evidence does not rebut these findings or rationale. Bennett, like Hayes, teaches transmitting time multiplexed signals to slave memory devices, and Bennett teaches slave memory devices ranging from the trivial to the complex. (*See* Bennett, col. 93, l. 64 to col. 94, l. 5; B4; B7.)

Rambus asserts that Bennett does not teach a single chip memory device. Claim 2 does not require a single chip. Assuming arguendo that it does, Rambus asserts that Bennett only teaches "that the VBI can be placed on the same VLSIC chip under certain circumstances, [but] it teaches away from doing so when the chip is relatively simple, like a memory device." (*See* Reopen Req. 15.)

Contrary to Rambus's single chip argument based on an asserted tendency toward complexity in Bennett, as quoted *supra*, Bennett

specifically contemplates "the pass[ing of] but a single bit of data from a single master device to a single slave device . . . . The *versatility* is from the *trivia*l to the profound." (B4 (emphasis added).)

Rambus's position that Bennett teaches only simple memory devices and teaches away from memory devices with an integrated interface (a VBI) (*see* Reopen Req. 20) also relies on Murphy's testimony that "[t]he same circuitry supports everything form 37-path embodiments to 3-path embodiments, the only difference being that portions of the interface may be disabled." (3rd Supp. Murphy Decl. ¶ 18.) This testimony and Rambus's position do not account for common sense possessed by skilled artisans and the breadth of claim 2. If circuitry on a memory device can be "disabled," skilled artisans would have figured out that only some of it would need to be put on a simple or trivial 3-pin memory devices to save the cost of putting it on that device and then disabling it. Claim 2 also does not preclude complex circuitry whether disabled or not.

Even though Bennett does discuss memory cards (*see* B3) as Rambus also maintains, Bennett points toward single chip memory devices (B1-B3). In any event, even Bennett's slave memory card, like Hayes's slave memory board, satisfies the broadly recited memory device in the claims as noted *supra*.

As indicated *supra*, the Board (*see* PTAB 2012-9762; PTAB 2012-2081, BPAI 2012-000168, and BPAI 2012-000169 decisions) and a District Court ("*Hynix II*")[6] have addressed the single chip argument and similar

[6] *Rambus, Inc. v. Hynix Semiconductor, Inc.* 628 F.Supp.2d 1114, 1132-38 (N.D. Cal. 2008) (Judge R. H. Whyte ruling on summary judgment and

arguments by Rambus in related proceedings. To the extent Rambus maintains the Board overlooks arguments made here, *Hynix II* and the above-listed decisions are adopted and incorporated herein by reference in response.

In *Hynix II*, Judge Whyte in made extensive factual findings and "concludes that the Manufacturers have carried their burden of producing evidence that Bennett discloses a memory device, and that Rambus failed to rebut this showing." *Hynix II* at 1131. Judge Whyte found that the Bennett inventors "were aware of memory cards and referred to them as such when they chose" and "disparaged the . . . 'many cards [that] can be placed on the bus.'" (*Id.* (quoting Bennett at col. 37, ll. 26-28).) Judge Whyte also found that the Bennett inventors turned away from such memory cards and toward "VSLIC devices, including memory devices" which the court referred to as "such memory chips." *Hynix II* at 1131.

As indicated in the description of Bennett *supra*, Bennett refers to "VLSIC chip devices" and states that "[m]any, if not most, applications of VLSIC technology are likely to include memory devices." (Bennett, col. 90, ll. 42-44; B2.) Bennett's "paramount object" is to provide flexible, versatile, and configurable communication between "very large scale integrated VLSI (circuit) elements" (col. 12, ll. 14-25) – i.e., "VLSIC chips" (col. 9, ll. 35-40). (*See* B1.) The term VLSIC (very large scale integrated circuit) in Bennett and conventionally signifies a single chip device. *See Rambus Inc.*

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anticipation by Bennett of similar claims 27 and 43 in the 6,314,051 patent which was also involved in the Board's BPAI 2012-000169 original and rehearing decisions).

v. Infineon Tech. AG, 318 F.3d 1081, 1085-86, 1091 (Fed. Cir. 2003) (defining Rambus's claim term, "integrated circuit device," as a "circuit constructed on a single monolithic substrate, commonly called a 'chip'") (relying on trade dictionaries, citations omitted). Bennett states that a VLSIC chip "cannot currently provide for as much memory as can be placed on a card" (col. 9, ll. 47-48), but "VLSIC technology promises much higher performance than that of cards," (col. 9, ll. 45-47), and "[t]he [VLSIC] technology is projected to drive signals from chip to chip in 20 to 40 nanoseconds" (col. 9, ll. 58-60; B4). (*Accord* AA 3.)

Rambus also contradicts itself by arguing that "extrinsic evidence also demonstrates that 'memory device' is a single chip that does not include a memory controller." (Reopen Req. 11.) If that extrinsic evidence is correct, then Bennett's "memory device" also signifies a single chip.[7] In other words, Bennett's disclosure of the same term, "memory device[]" (B2), references to "VLSIC upon the same chip substrate," "interfaces intended to be built with . . . Memory," (B1) and other similar references to VLSIC, chips or "same" substrates (B1-B4), combined with a limited and disparaging discussion of memory cards as prior art (B3), all show that Bennett's memory device includes a single chip embodiment (even if the term also signifies other memory forms of memory as Rambus argues). Bennett's Figures 1 and 38 also represent single chip memory devices. (*See* B1, B2.)

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[7] *See* note 5 *supra*, *In re Rambus Inc.*, 694 F.3d at 42 (holding that the claim term "memory device" in a related Rambus patent can signify but is not limited to a single memory chip and includes a memory board).

As discussed above, Bennett discloses ROM chips and implies other chips for reading and writing data, at least suggesting the popular DRAMs for reading and writing. Judge Whyte makes a similar finding:

> Bennett discusses ROMs while explaining the limited number of operations that can be done with a memory device, and it does so to point out that memories like ROMs cannot receive write operations. . . .*Bennett's discussion thus impliedly discloses some type of memory device that can receive write operations. The jury will have to determine at trial whether that implied disclosure encompasses a dynamic random access memory*.

Hynix II at 1137 (emphasis added).

Rambus also alleges that asynchronous RAS and CAS signals "perform completely different functions" in asynchronous systems like that of Hayes as compared to synchronous systems like those from Bennett, and thus, this shows the unobviousness of modifying Hayes's memory slave devices into either a synchronous memory board device or a synchronous memory single chip device. (*See* Reopen Req. 17 (discussing NVIDIA's expert Parris's Declaration).) But in Hayes, the CAS and RAS signals transfer within Hayes's slave memory device – a memory board device. (*See* Hayes Fig. 7 (showing internal portions of slave/memory board with RAS and CAS lines connecting RAM control logic 62 to the DRAM chips).) Moreover, to the processor chip in the Hayes external bus master, the memory board looks just like a single slave RAM chip. "An important feature of the present invention is that to local bus 17 master [i.e., processer 10 or chip 16, Hayes, col. 14, ll. 3-4)] there is no distinction between on-board RAM and off-board RAM." (Hayes, col. 14, ll. 29-31.) Therefore,

contrary to Rambus's arguments, the RAS and CAS signals on the memory board slave device do not overly complicate rendering such a device into a single slave chip device or render unobvious sending a synchronous signal to either one – especially since, as noted *supra*, Hayes's system sends time multiplexed signals from a master to a slave (which look the same to the bus master whether the slave is a board or a chip) as similarly occurs in Bennett.

Further, since Bennett similarly discloses memory boards and memory chips according to the record and Rambus, Bennett suggests the obviousness of synchronizing either one of these memory devices, including a memory device such as Hayes's memory board – i.e., regardless of the functionality of the RAS or CAS signals thereon. (*See also* Ex. Det. 7, 8 (addressing Rambus's arguments about RAS and CAS signals and relying on the Parris testimony showing the "shift in the art from asynchronous to synchronous systems" to increase speed).)

In sum, Rambus's contentions which rely on Murphy's new testimony add little or nothing to Murphy's prior testimony as the Examiner finds. (*See* Ex. Det. 5-6, 9 (finding that Murphy's Third Supplemental Declaration to be cumulative to prior testimony).) Rambus's further reliance on Dr. Jacob and Betty Prince also fails to show unobviousness.

Rambus asserts that Dr. Jacob and others such as Betty Prince show distinctions between asynchronous and synchronous devices and logic. Rambus's assertions do not overcome the Board's finding that skilled artisans were modifying asynchronous systems and transforming them into synchronous systems while keeping some of, or modifying, the logic in asynchronous systems, as the expert Parris testifies and as the Examiner finds in reliance thereon. (*See* Reopen Req. 18-19; Ex. Det. 6-14.)

Rambus cites to Dr. Jacob's textbook which describes a history of DRAMs. In the mid-1970's, "[o]ther early DRAMs were sometimes clocked . . . by a periodic clock signal" (i.e., apparently, synchronously) and then the technology moved toward asynchronous devices. (*See* Ch. 12, 461, § 12.2.2.) Dr. Jacob explains that asynchronous DRAM devices were "more of a hindrance than an asset" and that "computer manufacturers pushed to place a synchronous interface on the DRAM device." (*See id*. at 466.) (It is not clear when this "push" occurred or who the manufactures were, but Rambus relies on the textbook to support its position.)

In any event, Dr. Jacob states that a central difference between RAS and CAS in synchronous and asynchronous DRAMs is that the latter involves controlling "latches that are internal to the DRAM device" while the former involves

> signals [which] deliver . . . commands . . . acted upon by the control logic of the SDRAM device at the falling edge of the clock signal. In this manner, the operation of the state machine in the DRAM device moved from the memory controller into the DRAM device, enabling features such as programmability and multi-bank operation.

(*Id*.)

Rambus's assertions fail to show how Dr. Jacob's textbook reveals an insurmountable, if any, challenge, in accommodating any functional difference between synchronous and asynchronous RAS and CAS signals. Rambus also does not show that synchronously operated logic circuits including any "truth table[s]" discussed by Betty Prince would have presented any technical challenge to skilled artisans attempting to modify internal DRAM circuits to handle RAS and CAS logic. (*See* Reopen Req. 18 (discussing Betty Prince).)

Parris also contradicts Rambus's assertions and describes modifying, in a "straight forward" manner, i.e., "well within the ability of one of ordinary skill in the art," such "previously asynchronous DRAM ['RAS' and 'CAS'] signals" to be "on-chip," generally describes "incorporat[ing] asynchronous functionality on previous asynchronous memory systems into synchronous memory systems," and further notes that the "logic circuitry [including latches, registers, and counters] was typically [modified to be] . . . synchronous with the [external] clock". (Parris Decl. ¶ 9.)

Rambus also argues that the Board does not identify a reason for modifying Hayes's traditional asynchronous CAS and RAS signals to include Bennett's clocking scheme. But as the Examiner recognizes, the Board did identify reasons, including the industry push toward integration and synchronization to create smaller and faster memory devices. (*See* Ex. Det. 7 (citing '623 Bd. Dec. 29 which cites Parris Decl. ¶¶ 18-20).) Dr. Jacob's textbook and Rambus's other cited evidence fail to rebut Parris who also testifies as follows: "To the contrary [of Murphy's testimony and Rambus's arguments], adding logic on-chip with the memory device increases processing speed for multiple reasons, including reducing propagation delays and allowing the memory device to by physically closer to other devices driving the bus." (Parris Decl. ¶ 19.)

In addition, Hayes also discloses at least partial synchronization - bank select strobes on the memory board device are "synchronized with the processor timing by ARR RASIN (Array Row Address Strobe In)" during a memory board transaction. (Hayes, col. 23, ll. 38-41.) The evidence shows that synchronizing signals with an external clock would not have required an unobvious or insurmountable modification of the traditional RAS, CAS, or

DS signals in Hayes, contrary to Rambus's arguments - arguments which lack sufficient factual supporting evidence. (*See* Reopen Req. 16-18.)

Other alleged structural features in SDRAMs (synchronous DRAMs) supposedly showing unobvious according to Rambus, such as programmable registers and multiple internal banks, fail to support Rambus, because these added SDRAM features are neither needed to modify Hayes nor to satisfy the claims. (*See* Reopen Req. 19-20.) Rambus does not assert that it invented these SDRAM features, that synchronous memory devices require them, or that the claims require them, so it is not clear how the features show unobviousness. Bennett discloses synchronous memory chips that either have or do not have these specific SDRAM features – showing the obviousness of using generic synchronous memory chips encompassed by the claims.

Based on the foregoing discussion, Rambus's new evidence and arguments do not show unobviousness or error in the '623 Board Decision as the Examiner finds and reasons.

Hayes with Bennett and Inagaki – Claims 3, 4, 12, 13, 21, and 22

Rambus does not direct attention to a specific claim. Claim 3 is selected as representative. Claim 3 depends from claim 2 and additionally requires sampling first and second data portions on odd and even phases of the external clock signal. The record supports the Examiner's findings and rationale which are hereby adopted and incorporated by reference. (*See* Ex. Det. 10-14.) Rambus's new evidence does not undermine the '623 Board Decision. (*See* Bd. Dec. 29-31.) As the Decision explains and as noted *supra*, Hayes uses a clock to drive time multiplexed signals to a memory device. Bennett also uses a clock to drive time multiplexed signals and to

synchronize memory devices. Inagaki merely teaches using both clock phases, i.e., the rising and falling edges of an external clock, to double the clock speed in memory devices. (*See id*.)

As the Examiner recognizes, contrary to Rambus's characterization, Bennett's system is not being modified by the proposed combination, but rather, Bennett is employed to suggest using an external clock to synchronize memory devices. As such, as the Examiner recognizes, Rambus's argument and Murphy's testimony that Bennett's system would have been rendered inoperable or that Bennett's principle of operation would have been destroyed via the proposed prior art combination are not germane to the proposed rejection. (*See* Ex. Det. 12-13; Reopen Req. 24-25.)[8]

Contrary to related arguments by Rambus that Bennett's system would not have employed a faster clock (s*ee* Reopen Req. 24-25), Bennett's system is not being modified as noted, and in any event, contemplates faster speeds including doubled speeds: "The technology is projected to drive signals form chip to chip in 20 to 40 nanoseconds with internal gate delays of 1 to 2 nanoseconds." (B4; Ex. Det. 12 (also quoting this Bennett sentence).) This fact and related facts, including a universal desire for speed and industry drives toward integration, all suggest the obviousness of using a

[8] The Board addressed arguments about Bennett's alleged inoperability in a related decision involving Rambus. (*See e.g.*, PTAB 2012-001976 at 19-30).) The '1976 decision, adopted and incorporated herein by reference, finds that Bennett's principle of operation would not have been destroyed or that Bennett's system would not have required appreciable alteration to use falling and rising clock edges. In the alternative, the '1976 decision finds that Bennett's system would not require two clocks for simple single device systems.

both edges of a clock to gain clock speed in Hayes as modified by Bennett, according to Inagaki's teachings. As the '623 Board Decision also explains, in addition to increasing speed using both the rising and falling clock edges, Inagaki also suggests using a relatively slower clock's dual edges as a mere substitute for a faster clock which uses only the rising edges. Using dual edges can also allow for a decreased number of signal lines since twice the data can be pushed over half the lines using both clock edges as Inagaki teaches. (*See* Bd. Dec. 29-31.)

Based on the foregoing discussion, Rambus's new evidence does not show unobviousness and does not upset the '623 Board Decision as the Examiner finds and reasons.

Hayes with Inagaki – Claims 12 and 13

Claim 12, like claim 3 discussed *supra*, requires sampling data on both clock edges. Rambus does not direct attention to either claim 12 or 13. Claim 12 is selected as representative.

The Examiner's findings and rationale are supported and adopted and incorporated herein by reference. (*See* Ex. Det. 10.) Rambus maintains that the prior art combination does not render obvious a synchronous memory device using a data strobe and a periodic clock. (*See* Reopen Req. 26.)

Hayes's DS satisfies the data strobe signal as discussed *supra*, and Hayes and Inagaki each disclose a clock, contrary to Rambus's arguments. As the Decision explains – which Rambus does not address - claims 12 and 13 depend from claim 1, and unlike claim 2, do not recite synchronous operation. Inagaki's clock samples data during odd and even phases of a clock, as claim 12 requires: "'[S]ince one bit is output on each half-cycle, the operating speed is twice that of the conventional speed.'" (*See* '623 Bd.

Dec. 30 (quoting Inagaki at 4).) Rambus also does not provide new evidence to upset the '623 Board Decision. (*See* Reopen Req. 26.)

Assuming arguendo that the claims implicitly require synchronous operation, Inagaki characterizes the clock operation as synchronous: For example, "clock φ1 is generated synchronously with the external clock φ." (Inagaki at 5 (discussing Figure10).) As the Examiner also notes, the Parris declaration and other references of record show that such synchronous operation was known and the industry was moving towards it. (*See* Ex. Det. 14-15.) Using dual edges of a clock (synchronously or not) would have been obvious to increase speed as Inagaki teaches.

Based on the foregoing discussion, Rambus's arguments, lacking in new evidence, do not show unobviousness and do not upset the '623 Board Decision as the Examiner finds and reasons.

Hayes with Ohshima – Claims 2-10, 12-14, 16, 17, and 20-26

Rambus does not direct its arguments to any single claim. Claim 2 is selected to be representative of the above-listed group based on Rambus's arguments. The Decision largely relies on and refers to NVIDIA's *inter partes* request and Brief for the rejection of these claims. (*See* '623 Bd. Dec. 32-33.) As an example, NVIDIA relies on Ohshima to teach that intervening circuits should be added on-chip in a simple chip-to-chip interface. NVIDIA also relies on Ohshima's synchronous chip teachings and other features to increase speed in a DRAM. (*See e.g*. NVIDIA App. Br. Exhibit 14 (claim chart at 1.2, 2.0); App. Br. 13; I.P. Request at 30-35.) NVIDIA's *inter partes* request reasons that Ohshima teaches that combining logic on chip reduces the number of chips and complexity. (*See* I.P. Request at 30.) Rambus does not challenge these relied upon findings or rationale.

The Examiner reasons that incorporating the Hayes RAM control DS circuitry into a single chip memory device according to Ohshima's teachings would have been obvious and that the claims do not require incorporating all the RAM logic into a single chip as Rambus's arguments imply. (*See* Ex. Det. 15-16; Reopen Req. 27-28 (citing Murphy 3rd Supp. Decl. at ¶¶ 28-29).) Murphy's Third Supplemental Declaration addresses the obviousness of incorporating all the Hayes DS RAM logic into a single chip and thus fails to address the Board's Decision. (*See* '623 Bd. Dec. 32-33.) The thrust of Rambus's position reduces skilled artisans to automatons who would blindly incorporate all of Hayes's RAM control logic which controls multiple chips into a single chip. To the contrary, as a matter of routine skill, skilled artisans would have eliminated any unnecessary circuitry to create a single, simple DRAM chip having the necessary interface control to control that DRAM to transfer data as Ohshima shows.

Such a combination involving integration would have been obvious for creating faster and smaller components as Parris declares as noted *supra*. *See also Dystar Textilfarben GmBH & Co. Dutschland KG v. C.H. Patrick Co.*, 464 F.3d 1356, 1368 (Fed. Cir. 2006) ("[A]n implicit motivation to combine exists ... when the 'improvement' is technology-independent and the combination of references results in a product or process that is more desirable, for example because it is stronger, cheaper, cleaner, faster, lighter, smaller, more durable, or more efficient.") Contrary to Rambus's arguments (Reopen Req. 23), *Dystar's* motivation is not limited to "technology-independent" improvements. Rambus's arguments illogically would mean that the memory device industry or any single industry would not desire speed increases.

Ohshima teaches using "newly developed high speed DRAMs . . . and their innovative circuit techniques" to solve memory bottleneck problems. (*See* Ohshima 1303 ("Summary").) Ohshima also discusses using the "Rambus DRAM" for the same or similar purpose of increasing speed. (*See id.*) Rambus does not assert that Ohshima is not prior art in this reexamination proceeding. In several other proceedings before the Board, Rambus has asserted that their claimed devices have been highly successful to solve speed and memory bottleneck problems. Using these synchronous DRAMs and similar DRAMs to modify a single DRAM of Hayes while incorporating the Hayes DS logic to tell the DRAM that data is valid would have been obvious. As noted, Parris bolsters the obviousness of such integration and testifies that asynchronous systems were migrating to synchronous memory devices and designers were incorporating memory logic into such integrated devices to increase speed.

Based on the foregoing discussion, Rambus's new evidence and arguments do not disturb the '623 Board Decision as the Examiner determined.

Kushiyama with Hayes and Lu – Claims 1-14, 16, 17, and 19-26

Rambus does not direct its arguments to any single claim. Claim 1 is selected to be representative of the above-listed claims based on Rambus's arguments. As Rambus notes, the Examiner finds that Lu teaches incorporating logic circuits into memory, and finds that it would have been obvious to incorporate some of the Hayes RAM control logic, such as the DS signal circuitry, into a DRAM of Kushiyama. (*See* Reopen Req. 28.) As the '623 Board Decision explains:

> NVIDIA reasons that integrating the DS logic of Hayes into the Kushiyama chips would have been obvious where Lu teaches incorporating on-chip logic to make DRAMs more intelligent and to optimize performance at the system level. (Req. App. Br. 14-15.) Mr. Par[r]is corroborates this point and notes that chip designers were employing asynchronous circuits on-chip, including some strobe signals, like RAS and CAS, and that moving such circuits on-chip increase speed.

(‘623 Bd. Dec. 33 (citing Parris Decl. ¶¶ 9, 19.)

In response to the Board’s finding, Rambus maintains that the Board “provides no indication of how the DS signal from Hayes’s asynchronous system would have been incorporated into Kushiyama’s synchronous system or why such incorporation would have been beneficial.” (Reopen Req. 28-29.) But Rambus does not show that skilled artisans would have been unable to make such a change, and the DS signal serves the stated purpose in Hayes of telling the memory device that data is valid and thereby ready to be sampled, rendering its use in other memory devices to signal sampling obvious. (*See* Ex. Det. 17; *accord* Parris Decl. ¶ 11 (discussing a similar TrncvrRW signal and explaining why indicating valid data to a slave indicates when to sample); ¶ 24 (discussing Kushiyama).)

The record reflects that the skill level here in memory systems was advanced at the time of the invention. Hence, while Murphy testifies that such integration would be “non-trivial” and “the disadvantage of cost and establishing a common architecture may outweigh the advantages of new features” (*see* 3rd Supp. Murphy Decl. ¶31), this testimony falls short of showing that skilled artisans could or would not have seized the known

advantages. Rambus similarly reasons that artisans would not have incorporated asynchronous features into synchronous systems and that Lu does not "unequivocally teach integration of logic into DRAMs." (Reopen Req. 29 (citing 3rd Supp. Murphy Decl. at ¶¶ 31-32).)

Lu discusses trade-offs and implicit in trade-offs is a weighing process by skilled artisans. Rambus's evidence and arguments fail to show how weighing the Lu factors redounds to unobviousness. Lu explicitly states that "for some systems new functions, better performance, and size reduction can be achieved by integrating more logic circuits on DRAM chips." (Lu at 98.) Lu indicates that "high bandwidth[,] capacity" and "cost, reliability and packaging" must all be considered. (*Id*. at 99.) Higher cost does not mandate unobviousness. Faster, smaller, and more durable packages constitute universal motivators under *Dystar*. Integrating logic on-chip creates fewer chips and faster chips based on propagation distance and simplifies external wiring (reliability) and packaging. As Lu states, "ASIC DRAMs, adding logic functions on-chip with the memory, provide high density and high performance . . . . [since] [d]ata processing executed within one chip eliminates interface loss in speed and power consumption, which has been existing inevitably in combination of standard DRAMs with basic common functions and logic parts." (*Id*.)

Based on the foregoing discussion, Rambus's new evidence and arguments do not upset the '623 Board Decision as the Examiner finds.

Farmwald '755 with either of Lu or iRAM

Claims 1-4, 6-9, 11-13, 15, 16, 18-22, and 24-26

Rambus primarily focuses on independent claim 11, selected to be representative based on the arguments presented, even though independent claims 1 and 19 are broader than claim 11. Rambus maintains that the rejection is deficient because the TrncvrRW signal disclosed in Farmwald '755 does not "cause the memory devices to sample data" as required by the "strobe signal" recited in the independent claims. (Reopen Req. 31.) As the '623 Board Decision and the Examiner explain, the TrncvrRW signal indicates there is valid data on the bus, thereby indicating it is time to sample the valid data. (*See* '623 Bd. Dec. 34; Ex. Det. 20.)

The '623 Decision quotes Farmwald '755 as follows:

> Persons skilled in the art will recognize that a more sophisticated transceiver can control transmissions to and from primary bus units. An additional control line, *TrncvrRW can be bused to all devices on the transceiver bus*, using that line in conjunction with the Addr-Valid line to indicate *to all devices on the transceiver bus* that the information on the data lines is: 1) a request packet, *2) valid data to a slave*, 3) valid data from a slave, or 4) invalid data (or idle bus). *Using this extra control line obviates the need for the transceivers to keep track of when data needs to be forwarded* from its primary bus to the transceiver bus – all transceivers send all data from their primary bus to the transceiver bus whenever the control signal indicates the condition 2) above.

(Bd. Dec. 36-37 (quoting Farmwald '755 at col. 21, ll. 35-49) (emphasis supplied).)

The TrncvrRW signal, as quoted *supra*, indicates "to all [slave] devices" that there is "valid data to a slave" and thereby signals the slave

device to sample the data – because the data is valid and ready. As the passage *supra* reveals, the TrncvrRW "extra control line obviates the need for the transceivers to keep track of when data needs to be forwarded."

Tellingly, Rambus's new argument that the TrncvrRW signal in Rambus's '755 patent does not function as a "strobe signal" as recited in the independent claims constitutes a pronounced shift from the thrust of Rambus's original position as presented in its Respondent Brief. Rambus's arguments originally did not focus on the new allegation here that the TrncvrRW fails to function as the strobe signal recited in the claims.

Rather, Rambus's central contention addressed in the '623 Board Decision was that "NVIDIA . . . mischaracterizes Farmwald '755 by claiming 'all devices on the bus receive the TrncvrRW signal" (Rambus Resp. Br. 26) and similarly that "there is no reason one would have modified a memory device to receive a signal that is specific to a transceiver." (Rambus Resp. Br. 24.)

In essence, Rambus originally maintained that Farmwald '755 did not disclose or render obvious sending a TrncvrRW strobe signal to a single chip memory device or integrating a memory stick which receives that strobe signal into a single chip. Based on NVIDIA's proposed rejection, Rambus's contentions, and the Examiner's findings, the Board concentrated the bulk of the Farmwald' 755 analyses on those paramount issues before it. (*See* Bd. Dec. 38-44.)

Rambus's Request to Reopen quotes only the highlighted sentence below from Rambus's Respondent Brief, but Rambus relies on that sentence and maintains that the Respondent Brief shows that Rambus did not concede that the TrncvrRW signal functions as the claimed strobe signal:

> Even if the Board considers NVIDIA's argument, it should affirm the CRU panel on the merits. NVIDIA cites iRAM for motivating the same combination-moving the Farmwald transceiver on-chip--argued in issue 8. Here again, NVIDIA does not rebut the substantial evidence presented to the CRU showing how Farmwald '755 teaches away from this combination and how the *TrncvrRW does not function as the claimed strobe signal*.

(*See* Response 31 (quoting only the emphasized portion from Rambus Resp. Br. at 29) (emphasis added by Board).)

Rambus did not explain to the Board in its Respondent Brief why the TrncvrRW does not function as a strobe signal and did not point the Board to any rationale or evidence supporting the reason behind the denial. Such a "naked assertion" amounting to a denial that the Farmwald '755 does not function as a strobe signal, without explaining why, generally constitutes a waiver of the argument in typical appeals before the Board. *See In re Lovin*, 652 F.3d 1349, 1357 (2011).

As opposed to only truncated arguments as involved in *In re Lovin*, the thrust of Rambus's position essentially buried the naked assertion and pointed the Examiner, NVIDIA and the Board in a totally different direction which required some effort to analyze.[9] As a procedural matter, Rambus's

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[9] Rambus also refers to its "12/22/09 Response to ACP at 16-19" in an effort to show that it earlier raised this argument about the function of the TrncvrRW signal, but that response was not cited in its Respondent Brief (*see* Reopen Req. 31), and even if it were, it too concentrates on the same argument addressed in the '623 Board Decision – i.e., that a single memory chip in Farmwald '755 would not receive such a TrncvrRW signal.

For example, the "Response to ACP" summary arguments follow:

new evidence and arguments about the *function* of the TrncvrRW function fail to respond to the thrust of the new ground of rejection which concentrated on the *use* of the TrncvrRW signal in a single chip device. As such, Rambus's new position does not appear to be proper procedurally because it is not responsive to the thrust of the new grounds of rejection. But Rambus's new argument is made on remand before the Examiner and involves the same claim element in dispute prior to remand, the TrncvrRW signal, a situation not involved in *In re Lovin*. To avoid procedural pitfalls, the Board considers Rambus's new argument. *See Rexnord Industries, LLC v. Kappos and Habasit Belting, Inc*. No. 2011-1434 (Fed. Circ. Jan. 23, 2013) (holding that prior consistent positions in the record by an appellee in a reexamination proceeding are not waived and must be considered), http://www.ipo.org/AM/Template.cfm?Section=Federal_Circuit_Opinions &ContentID=35527&template=/CM/ContentDisplay.cfm.

Rambus's new evidence and arguments do not support this shifted argument. For example, Rambus argues that the '353 patent disclosure implies a "'data transfer start information'" requirement in claim 11, but Rambus does not explain how that disclosure limits further the recited requirement in claim 11 for the "strobe signal to initiate sampling" and why

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> In teaching these non-transceiver device [i.e., single chip] systems, the TrncvrRW or any equivalent signal is never used. Therefore, a person of skill in the art would understand that the '755 patent teaches away from using such a signal, except in combination with a transceiver device that connects to a transceiver bus on one end and a primary bus on the other end.

(Response to ACP at 19 (Dec. 22, 2009).)

that type of information, if it is imputed to be a claim limitation, distinguishes over the '755 Farmwald TrncvrRW signal. (*See* Reopen Req. 31 (quoting '353 patent, col. 8, l. 61).) A similar argument is addressed *supra* in the section discussing anticipation by Hayes. As discussed, column 8 does not describe *sampling* which claim 11 requires. Rather, it describes *transmitting* data *from* a memory device at two different delay times after the strobe signal and indicates that transmitting times relative to the strobe are governed by something other than the disclosed data strobe. Hence, it is not clear how the passage even applies to sampling or how it limits it even if it does apply. The TrncvrRW signal logically contains "data transfer start information" since it indicates valid data to a slave after which the memory device begins to sample the data.

In a related finding, the '623 Board Decision finds that "the '353 patent describes a delay between the strobe signal and sampling" and that "Rambus corroborates NVIDIA's point and describes a similar delay between the data and the strobe." (*See* '623 Bd. Dec. at 22; P.O. Cr. App. Br. 10; Req. Resp. Br. 12.) Rambus does not challenge this finding or explain how the disclosed start information at column 8 upsets it. As discussed, some delay in clock cycles not defined by the strobe signal occurs between sampling and the strobe signal as disclosed and claimed in the '353 patent. In light of this unchallenged delay between the strobe signal and sampling, Rambus fails to demonstrate how the TrncvrRW signal (like the Hayes DS), as construed here, is inconsistent with the '353 Patent Specification's strobe signal.

Also, Parris's testimony supports the Board and directly contradicts Rambus: "[T]he TrncvrRW signal does indeed indicate when the memory

device is to begin sampling write data." (Parris Decl. ¶ 11 (explaining, *inter alia*, that "[t]he slave should not, and will not, begin sampling write data until the data is valid.").) Rambus fails to present persuasive evidence rebutting Parris's testimony or the evidence in Farmwald '755 relied upon by the Board and the Examiner. Murphy testifies that because the "TrncvrRW signal indicates whether a transceiver should forward data," the signal would not be sent to a memory device "since the memory device does not make the forwarding decisions that are made by a transceiver." (3rd Supp. Murphy Decl. at ¶ 35.)[10] Murphy's testimony focuses on whether the TrncvrRW signal is sent to a single chip and does not squarely address the function of the signal. It also seemingly contradicts, without a supporting explanation, the un-rebutted fact, discussed further below, that "all devices" (including memory devices) on the transceiver bus receive the TrncvrRW signal (i.e., not just memory stick devices with transceivers thereon) to indicate valid data to a slave device.[11]

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[10] Rambus also argues that "the purpose of the TrncvrRW signal is to allow the transceiver to decide whether to forward data from the transceiver bus to the primary bus." (Reopen Req. 31.) An interface on a DRAM chip obviously can serve the same function. Rambus also notes that the signal indicates forwarding data the other way – from the primary bus to the transceiver bus. (*See id*.) The Board agrees with Rambus that the TrncvrRW signal logically indicates to a slave to send or receive data both ways – i.e., depending on if a read or write is being performed.

[11] The memory stick, or primary bus unit, includes a transceiver device 19 and one or more memory chip devices. (*See* Reopen Req. 30 (annotating Fig. 9 of the '755 patent and showing the memory stick and external transceiver bus); '623 Bd. Dec. 35 (FW6), 40.)

Rambus does not direct attention to another signal in its '755 Farmwald patent which would cause data sampling and which occurs after the TrncvrRW signal. Rambus does not maintain that data sampling does not occur after the TrncvrRW signal as Parris's testimony shows. (Parris Decl. ¶ 11.) As such, Rambus fails to define to a patentable distinction between the two signals. Even if the TrncvrRW signal somehow does not constitute a strobe signal, using it as such a signal to tell the memory device to start sampling because the data is valid would have been obvious for the reasons noted- i.e., the data is ready to be sampled.

Rambus's new thrust about the TrncvrRW functionality may have been in anticipation of the later-decided controlling precedent, *In re Rambus* (*supra* note 5), holding that the term "memory device" in the family of Rambus's patents is a generic term that embraces memory board devices and memory chip devices. However, this rejection was not proposed in NVIDIA's original *inter partes* request and the Board did not propose it as a new ground.[12]

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[12] Also, *In re Rambus* indicates that a portion of the Board's underlying analysis in that case was "incorrect" for "*equating* the multichip 'memory stick' with a' memory device,'" but the court held that "this does not mean that a memory device must contain only one chip." 694 F.3d at 47 (emphasis added). The court held that a "'memory device' is a broad term which has been used consistently in the '918 patent and in the family of patents related to it to *encompass* a device having one or more chips." *Id*. at 48 (emphasis added). Hence, while the court found that "a memory device and a memory stick are [not equated or not] the same," *see id*. at 47, since a memory device includes multiple chips and includes the prior art "iAPX Manual's memory module, which contains several chips and a controller that provides the logic for those chips to function," *id*. at 50, it appears that the

The TrncvrRW signal in Farmwald '755 is sent to *all memory devices* (i.e., including single chip memory devices) on the external (i.e., transceiver) bus as the Board finds. ('623 Bd. Dec. 39-40.) For example, as the '755 patent states, "'[a]n additional control line, TrncvrRW can be bussed to *all devices on the transceiver bus*.'" ('623 Bd. Dec. 36 (quoting Farmwald '755 at col. 21, ll. 37-39).) The '755 patent also describes "'memory devices *on the transceiver bus* as well as on primary bus units.'" (*See* '623 Bd. Dec. 36, 39 (quoting '755 Farmwald at col. 21, ll. 6-7 (emphasis added).)

Rambus now virtually concedes this point, contrary to its earlier Respondent Brief position. For example, Rambus now states that the TrncvrRW signal "can be bused to *all devices* on the *transceiver* bus. Nothing in the specification suggests that the TrncvrRW signal is also sent to devices on the primary bus." (Reopen Req. 33 n.10 quoting Farmwald '755 at col. 21, ll.37-39 (first emphasis by Board).) Rambus's second quoted sentence sets up a straw man. The *primary* bus on the memory stick

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generic term "memory device" also includes the two disclosed species – i.e., the memory stick device and a memory chip device – even though they are not "the same" species. Alternatively, perhaps the court carved out an exception from the broad reach of the term "memory device" so that it somehow includes everything from a broad prior art memory board to a narrow single chip memory device except the intermediate memory stick. *See id*. at 48 ("the specification could not be clearer that the disclosed invention can be practiced with either a memory device or with a memory stick.") If so, the court did not have benefit of the explicit finding by the Board in the '623 Board Decision and concession by Rambus here that the TrncvrRW signal is bussed to all memory devices on the transceiver bus (i.e., to memory stick devices and memory chip devices on that bus). (*See* '623 Bd.Dec. 39.)

has nothing to do with the Board's rejection or Rambus's concession. All devices, including single chip memory devices, disclosed in the '755 patent as residing on the external *transceiver* bus, receive the TrncvrRW signal. As the '623 Board Decision explains, and as Rambus depicts (*see* Reopen Req. 30), the transceiver bus is the bus external to the memory stick and that bus has memory sticks and other memory devices attached to it. (*See* note 11.)

Rambus similarly concedes the point that the TrncvrRW signal goes to all memory devices in another argument. "Because it [the TrncvrRW signal] does not indicate to which *memory device* data being transmitted is intended to be written and is provided to *all devices* on the transceiver bus, TrncvrRW cannot be considered to indicate to a *memory device* to initiate sampling." (Reopen Req. 31 (emphasis supplied).)

Rambus concession quoted *supra* imbeds an unclear argument which is difficult to address, but Rambus appears to be taking the untenable and immaterial position that each "memory device" disclosed in its '755 Farmwald patent cannot determine from the TrncvrRW signal that it is being addressed by a controller for a data transfer. This argument is a red herring because the Board does not assert that the TrncvrRW signal includes address information and the claims do not require it. Perhaps Rambus implies that the TrncvrRW signal goes to all slave memory devices on the transceiver bus as a broadcast signal. (*See e.g.* '353 patent, col. 16, l. 49 *et seq*. (discussing broadcast data).) If so, claims 1, 11, and 19 do not preclude all the memory devices on the '755 Farmwald transceiver bus from sampling the data on the bus in response to the TrncvrRW strobe signal.

Assuming for the sake of argument that Farmwald' 755 only discloses that the TrncvrRW goes to a transceiver chip on a memory stick to indicate

valid data to that slave memory stick device, as the Decision and the Examiner explain at length, the prior art combination, which includes Farmwald '755 with either of Lu or iRAM, renders obvious modifying the stick by integrating its simple functionality into a single chip memory device having a transceiver interface. An obvious purpose would have been that receiving a TrncvrRW signal or a similar strobe signal (assuming arguendo that the TrncvrRW signal does not satisfy the strobe signal limitation for some reason) in a smaller and faster device such as a single chip would have informed the fast chip when to sample data since the TrncvrRW signal tells all *slave* memory devices that there is "2) valid data to a slave" (quoted *supra* from '755 Farmwald). (*See* Ex. Det. 22-24; Bd. Dec. 38-45.) As an example of further rationale for creating a single chip out of two chips, aside from the beneficial reduction in chip number, the Board reasons that Farmwald '755 specifically teaches that "'each teaching of this invention which refers to a memory device can be practiced using a [memory stick – i.e., a] transceiver device and one or more memory devices.'" (Bd. Dec. 36, 40 (FW7 quoting '755 Farmwald at col. 21, ll. 7-10).)

The Examiner's responses to Rambus, which rely on the '623 Board Decision, persuasively rebut Rambus's remaining arguments, add additional supporting facts and rationale, and are adopted and incorporated by reference as indicated at the outset. (*See* Ex. Det. 18-24.) For example, Murphy opines that combining a DRAM with a transceiver would make the DRAM chip bigger and hence slower than a normal DRAM chip, thereby defeating one rationale for obviousness. (*See* 3rd Supp. Murphy Decl. at ¶ 36.) However, that rebuttal compares the wrong devices, two chips, instead of a chip and a memory stick. A single chip memory integrated with a

beneficial transceiver interface would be smaller and faster than the Farmwald '755 multi-chip memory stick. A memory stick is "quite simple in function" ('755 Farmwald, col. 21, l. 18) and encompasses as few as two chips, a memory chip, and a transceiver chip which functions as a simple interface to the bus for the memory chip, further suggesting integration thereof. (*See* '755 patent col. 2ll. l8-24; Ex. Det. 23-24; '623 Bd. Dec. 41-45.)

Pursuant to the foregoing discussion, Rambus's evidence and arguments do not support altering the '623 Decision and the Examiner's Determination that claims 1-4, 6-9, 11-13, 15, 16, 18-22, and 24-26 based on Farmwald '755 and Lu or iRAM would have been obvious.

DECISION

Rambus has not shown that the Board's Decision, BPAI 2011-010623, requires a modification with respect to the affirmance of claims 1, 5, 7, 11, 14, 19, and 23 as anticipated based on Hayes.

Rambus also has not shown that Board's Decision, BPAI 2011-010623, requires a modification with respect to altering the underlying holding that the new grounds of rejection listed *supra* render claims 1-26 obvious.

Requests for extensions of time, if available in this *inter partes* reexamination proceeding, are governed by 37 C.F.R. § 1.956. *See* 37 C.F.R. §§ 41.77 and 41.79.

<u>REHEARING RELIEF DENIED and DECISION UNMODIFIED</u>

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