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BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte RAMBUS, INC.

Appeal 2012-009762
Reexamination Control No. 90/011,005
United States Patent 6,324,120 B2
Technology Center 3900

Before HOWARD B. BLANKENSHIP, KARL D. EASTHOM, and STEPHEN C. SIU, *Administrative Patent Judges*.

EASTHOM, *Administrative Patent Judge*.

DECISION ON APPEAL

Appellant, Patent Owner Rambus, Inc., appeals under 35 U.S.C. §§ 134(b) and 306 from the Examiner's decision to finally reject claims 26 and 29. Claim 33 has been confirmed. (App. Br.iii, vii.) We have jurisdiction under 35 U.S.C. §§ 134(b) and 306.

We AFFIRM.

STATEMENT OF THE CASE

Rambus refers to several related judicial and other proceedings including *inter partes* and *ex parte* reexaminations, International Trade Commission proceedings, and Federal District Court and Circuit Court proceedings in its Appeal Brief. (App. Br. iii-vii.)

Rambus appeals the Examiner's decision to maintain the rejections of claims 26 and 29 as obvious based on the combination of Bennett[1] and Fujishima[2].

The appealed claims follow:

26. A synchronous dynamic random access memory device having at least one memory section including a plurality of memory cells, the memory device comprising:

clock receiver circuitry to receive an external clock signal;

input receiver circuitry, including a first plurality of input receivers to sample block size information synchronously with respect to the external clock signal, wherein the block size information defines an amount of data to be output by the memory device in response to a first operation code; and

[1] Bennett et al., U.S. 4,734,909 (Mar. 29, 1988).
[2] Fujishima et al., U.S. 5,266,147 (July 6, 1993).

a plurality of output drivers to output the amount of data in response to the first operation code.

29. The memory device of claim 26 wherein the input receiver circuitry samples the first operation code synchronously with respect to the external clock signal.

ANALYSIS

The claimed invention involves a synchronous dynamic random access memory device - a synchronous DRAM. The '120 patent refers to DRAMs, and other memory devices, including RAMs and ROMs (read only memories) as "conventional." ('120 patent, col. 1, ll. 50-56.) Claim 26 requires a synchronous DRAM which can receive an external clock signal and a block size synchronously with that clock signal, wherein the block size information defines an amount of data to be output by the memory device in response to a first operation code. Rambus contends, *inter alia*, that the Examiner erred in finding that the combination of Bennett and Fujishima teaches or renders these features obvious. (*See* App. Br. 1.)

Bennett's Teachings

B1. Bennett's "paramount object" is to provide communication between "very large scale integrated VLSI (circuit) elements" (col. 12, ll. 14-18) – i.e., "VLSIC chips" (col. 9, ll. 35-40). Bennett discloses combining Versatile Bus Interfaces (VBI) and VLSIC "*upon the same chip substrate as the VLSI User Device*" (col. 12, ll. 29-32 (emphasis added)) with such a user device including "*interfaces intended to be built with* a CPU, IOC or *Memory*, or similar User device for signal or data exchange"

(col. 35, ll. 59-61 (emphasis added)). (*See also* col. 14, ll. 19-24 (describing "interface to the user devices (usually upon the same chip substrate)".)

Bennett's Figure 1 represents a single chip User Device, which includes memory, as noted *supra*: "Each Versatile Bus Interface Logics, for example Versatile Bus Interface Logics 102a, interfaces a User module, for example VLSI Circuit User Device 106a which is pictorially represented in shadow line within FIG. 1 *as existing on the same VLSIC chip substrate* as Versatile Bus Interface Logics 102a." (Col. 36, ll. 19-24 (emphasis added).)

Bennett's chips have up to 120 pins as a practical limit. (Col. 9, ll. 60-61.) Bennett also discloses different memory types as "Fast Memory" or "Large Memory" with the memory having address widths of 16, 24, or 32, and one fast memory embodiment having 37 pins (col. 92, ll. 15-56; Fig. 32). One large memory has at least 16 pins to access 2^{32} addresses by employing two 16-bit address words over successive clock cycles. (*See* col. 95, ll. 59-60; Fig. 36.)

B2. Figure 38 shows "memories device" 3802c and 3802d connected to a "Versatile Bus." (Col. 97, ll. 8-10.) In the next paragraph, Bennett refers to "VSLI chips hav[ing] access to all Versatile Bus lines and therefore, the Versatile Bus protocols." (*Id*. at ll. 20-22.)

Bennett elsewhere refers to "memory devices" including, but not limited to, a ROM: "Not all memory devices can perform all operations; for example, read only memory (ROM) cannot execute the write operations." (Col. 90, l. 66 to col. 91, l. 2.) Bennett then refers to "[s]ample memory operations in the following paragraphs" (col. 91, ll. 4-5) and thereafter describes "relatively small fast memories, and . . . larger and relatively slower memories" (col. 92, ll. 13-14).

Bennett also refers to "VLSIC chip devices" (col. 90, ll. 38-41) and in the next section, Section "4.1, Sample Memory Operations," states that "[m]any, if not most, applications of VLSIC technology are likely to include memory devices." (Col. 90, ll. 42-43.) Bennett generally discusses these chip devices as employing the interconnection protocol standards outlined generally in Section 3 and more specifically discusses memory devices in Section 4, including embodiments or configurations involved in Figures 31-36. (*See id*. at ll. 36-41.)

For example, as discussed in Section 4 of Bennett, Figures 32 and 33 represent fast memory read or write operations, with Figures 32 and 33 respectively signifying "DATA" transmission on 16 and 8 pins. Other pins are used for arbitration and slave ID. (*See* col. 93, l.12 - col. 94, l. 56.) Figure 36 represents pin designations and timing for a write operation to a large memory device with a 4315335 protocol "configuration." (*See* col. 26, ll. 54-57.) Figures 25a-h, represent more generic slave device configurations as discussed in Section 3 of Bennett. (Col. 25, l. 58 to col. 26, l; *see generally* columns 81-88).

B3. In addition to chips, Bennett also discusses memory cards in Section 2, "Description of the Prior Art" (*see* col. 5, l.52 *et seq*.), and states that "the functionality of VLSIC chips is often similar to cards today" but that "VLSIC technology promises much higher performance than that of cards," even though cards hold more memory and chips have higher development costs. (Col. 9, ll. 43-56.) In the next passage, Bennett discusses creating larger chips to accommodate a greater numbers of pins. (Col. 9, l. 66 to col. 10, l. 29.)

B4. Bennett describes a "third physical objective" – the VBI (versatile bus interface) "should occupy a reasonable VLSI circuit substrate area" using fast and efficient CMOS technology as the preferred embodiment. (Col. 13, ll.18-23.) Typically, only about 20 VLSIC devices will be interconnected. As a "first logical object," the VBI logics "should offer a fixed format, simply controlled, powerfully featured interface to the user devices (usually upon the same chip substrate)" yet with certain options for use. (Col. 14, ll. 20-30.)

Bennett contemplates simple devices with "as few as three pins" (Bennett, col. 12, l. 61), or "pass[ing] but a single bit of data from a single master device to a single slave device . . . [or more bits and devices]. The versatility is from the trivial to the profound." (Col. 15, ll. 26, 42-50.) Figure 32, a "sample fast memory," has "an address field arbitrarily sized at four bits." (Col. 93, ll. 13, 23.) Generally, large memories are slower than, and have more address pins, than fast memories. (Co. 94, ll. 26-33.) Bennett mentions that for large memories, "[a]ddress width may be configured to 16, 24, or 32 bits to match requirements." (Col. 94, ll. 35-36.) In another section, Bennett describes a fast memory which may have 16 bit words, and if so, "at a 40 nanosecond pace may either have to be very wide or very fast or both." (Col. 89, ll. 30-32.) "The technology is projected to drive signals form chip to chip in 20 to 40 nanoseconds with internal gate delays of 1 to 2 nanoseconds." (Col. 9, ll. 57-60.)

B5. Figures 25a-h, described in section 3 of Bennett, depict timing diagrams for slave devices on the VLSIC bus which have eight Configuration Parameters (e.g., 122123XX) stored in the devices. (*See* col. 86, ll. 31-32.) Bennett refers to the Section 3 figures as representing chips:

"Section 3 provided for the electrical connection of many chips on one bus . . . . Each chip recognizes the existence of the transactions . . . ." (Col. 90, ll. 27-30.)

Figures 25a-h, similar to Figures 35 and 36, show an ID/FUNCTION command, which includes a read or a write (*see e.g*. Fig. 35, 36).[3] (*See* col. 85, l. 9 to col. 87, l. 6.). Figure 34 shows multiple functions in a memory write code: i.e., a read-modify-write code signifying multiple functions in a single code.

B6. Bennett discloses synchronous clocked communication between bused VLSIC chips over 16 data lines at 25MHz, and notes that synchronous communication is more efficient than asynchronous communication. (Col. 13, ll. 3-17; col. 66, l. 9 – col 67, l. 18; col. 101, ll. 50-54 ("all communication . . . is synchronously referenced"); col. 102, ll. 9-27.) Bennett also states that the clock signals "are normally synchronous." (Col. 274, l. 62.)

B7. Bennett employs a dual-phase clocking scheme. (*See* Fig. 84.)

B8. As noted *supra*, Bennett contemplates simple systems having "a single slave memory." (Col. 57, l. 57.) Bennett explains that "the number of [device] locations strongly affects complexity." (Col. 8, ll. 30-31.) Bennett distinguishes between slaves and masters: slaves "only respond to

[3] Bennett also refers to functions as operations, which include read or write operations. (*See* col. 91, l. 62 to col. 92, l. 8; col. 91, ll. 43-53 ("functional operations"); Figs. 31, 35, 36.) Address data and operation codes may be sent as part of the "Slave Identification/Function information" cycle, "but this need not be so. The sample memory may receive this 'function' information as data." (Col. 90, ll. 54-58.)

information on the interconnect," masters "control the interconnect"; thus, slaves are subordinate to masters. (Col. 8, ll. 30-41.)

DRAM

Rambus maintains that employing a DRAM chip as one of Bennett's memory devices would not have been obvious. (*See* App. Br. 1, 6-18.) Rambus bolsters its argument by stating that Bennett does not disclose a synchronous single chip memory device. (*See, e.g.*, App. Br. 8-9.)

Rambus fails to show error in the Examiner's findings and rationale. The Examiner relies on Fujishima to show that DRAM chips were well known and on Bennett to teach single chip synchronous memory devices to support the obviousness of using a DRAM chip in place of one of the generic memory chips disclosed by Bennett. (*See* Final Office Action 4-7 (Aug. 26, 2011) ("FOA").) For example, as the Examiner finds, Bennett's "VBI [(Versatile Bus Interface)] is designed to be integrated <u>with each memory chip</u>." (FOA 5.) As another example and as the Examiner also finds, "the teachings of Fujishima show that . . . DRAMs were well known and commonplace." (FOA 6.)

Further, the '120 patent admits that "conventional" DRAM chips were "the most widely used" type of memory device. ('120 patent, col. 1, ll. 50, 52-53.) As Rambus acknowledges, the Board found in a related decision that "'DRAMs were a well-known, if not dominant, form of a memory chip device at the time of the invention.'" (*See* App. Br. 6 (citing Reexamination Control Nos. 95/000,178 & 95/001,152 and implicitly referring to the Board's BPAI 2011-009664 decision at 15) (Jan. 19, 2012).) Rambus does not dispute the finding that DRAM chips were dominant and popular chips at the time of the invention.

Contrary to Rambus's arguments, Bennett discloses a synchronous clocked single chip memory device (B1-B8) and at least renders a synchronous DRAM chip obvious, as the Examiner finds. As discussed further below, Bennett discloses read/write memory devices and notes that some chips, ROMs, do not perform writes (B4), thereby implying popular DRAM chips which do perform reads and writes.

The Board and a District Court ("*Hynix II*")[4] have addressed the single chip argument and similar arguments by Rambus in related proceedings. The related findings and rationale in *Hynix II*, and the Board's PTAB 2012-2081, BPAI 2012-000168 and BPAI 2012-000169, including the rehearing decisions involved in those reexaminations, are adopted and incorporated herein by reference.

Judge Whyte in *Hynix II* made extensive factual findings and "concludes that the Manufacturers have carried their burden of producing evidence that Bennett discloses a memory device, and that Rambus failed to rebut this showing." *Hynix II* at 1131. Judge Whyte found that the Bennett inventors "were aware of memory cards and referred to them as such when they chose" and "disparaged the . . . 'many cards [that] can be placed on the bus.'" (*Id*. (quoting Bennett at col. 37, ll. 26-28).) Judge Whyte also found that the Bennett inventors turned away from such memory cards and toward

[4] Attached as Exhibit O-3 to Rambus's Appeal Brief and reported as follows: *Rambus, Inc. v. Hynix Semiconductor, Inc.* 628 F.Supp.2d 1114, 1132-38 (N.D. Cal. 2008) (Judge R. H. Whyte ruling on summary judgment and anticipation by Bennett of similar claims 27 and 43 in the 6,314,051 patent which was also involved in the Board's BPAI 2012-000169 original and rehearing decisions).

"VSLIC devices, including memory devices" which the court referred to as "such memory chips." *Hynix II* at 1131.

As indicated in the description of Bennett *supra*, Bennett refers to "VLSIC chip devices" and states that "[m]any, if not most, applications of VLSIC technology are likely to include memory devices." (Bennett, col. 90, ll. 42-43; B4.) Bennett's "paramount object" is to provide flexible, versatile, and configurable communication between "very large scale integrated VLSI (circuit) elements" (col. 12, ll. 14-25) – i.e., "VLSIC chips" (col. 9, ll. 35-40). (*See* B1.) The term VLSIC (very large scale integrated circuit) in Bennett and conventionally signifies a single chip device. *See Rambus Inc. v. Infineon Tech. AG*, 318 F.3d 1081, 1085-86, 1091 (Fed. Cir. 2003) (defining Rambus's claim term, "integrated circuit device," as a "circuit constructed on a single monolithic substrate, commonly called a 'chip'") (relying on trade dictionaries, citations omitted). Bennett states that a VLSIC chip "cannot currently provide for as much memory as can be placed on a card" (col. 9, ll. 47-48), but "VLSIC technology promises much higher performance than that of cards," (col. 9, ll. 45-47), and "[t]he [VLSIC] technology is projected to drive signals from chip to chip in 20 to 40 nanoseconds" (col. 9, ll. 58-60; B11). (*Accord* AA 3.)

In other words, as *Hynix II* finds, Bennett turns to memory chips in place of memory cards. Addressing Rambus's expert Murphy's opinion that Bennett's 32 address and word bits would signify a room full of memory cards at the time of Bennett (1982), and not a chip, Judge Whyte found that "this 'large memory' is meant to illustrate the flexibility of the bus interface, not to suggest that Bennett contemplates that all memory devices designed for use in its system should be so large." *Hynix II* at 1130. The court also

recognized that Bennett teaches operating with as few as three VBI interface pins and minimizing the number of node pins; hence, the court reasoned that Murphy improperly focuses on the 32 bit example and other examples involving a larger number of pins. *See id*. at 1130-1131.

Rambus and Murphy here do not assert that Bennett's 32 address and word bits signify a room full of memory cards as they did in *Hynix II*. Rambus now asserts that Bennett's large memory signifies "a large number of memory chips on memory cards." (App. Br. 8 (citing Murphy Decl. ¶ 16).) Murphy does not set forth the basis for his new position or explain why it differs from his earlier *Hynix II* position. In any event, similar to findings to *Hynix II*, Bennett discloses "<u>up to</u> 2^{32} addresses of 32 bit words" (Bennett, col. 95, ll. 59-64 (emphasis added)) which includes single chip memory devices.

The record shows that Bennett contemplates a wide variety of pin number[s] (i.e., address and word bits) to replace cards. (*See* B4.) Bennett also discloses the option of passing "but a single bit of data from a single master device to a single slave device." (Bennett, col. 15, ll. 43-44.) Bennett also discloses 16 bit words in a large memory slave device and discusses faster memory devices having fewer pins. (*See* B4.) Rambus's argument that in Bennett's time frame, that even Bennett's fast memory embodiment also would have required multiple chips (*see* App. Br. 9 (citing Murphy Decl. ¶ 17), fails to overcome Bennett's specific disclosures related to single substrate chips. (*See* B1-B4; AA 3, 11-13.) Also, notwithstanding what Murphy contends existed in Bennett's time frame, Bennett "projected . . . chip to chip speeds in 20 to 40 nanoseconds." (B4.) Such chip speed projections do not preclude or render unobvious advances in DRAM chip

speeds. Rambus similarly fails to rebut the corresponding *Hynix II* rationale that Bennett discloses a versatile and flexible system not limited to any particular memory chip embodiment.

Rambus's also contradicts itself by arguing that "a person of ordinary skill in the art would understand . . . a 'memory device' to be a chip" (App. Br. 7 (citing Murphy Decl. ¶ 17).) If that understanding is correct, then the same skilled artisans would understand Bennett's "memory device" to embrace a single memory chip.[5] In other words, Bennett's disclosure of the same term, "memory device[]" (B2), references to "VLSIC upon the same chip substrate," "interfaces intended to be built with . . . Memory," (B1) and other similar references to VLSIC, chips or "same" substrates (B1-B4), combined with a limited and disparaging discussion of memory cards as prior art (B3), all show that Bennett's memory device includes a single chip embodiment (even if the term also signifies other memory forms of memory as Rambus argues). Bennett's Figures 1 and 38 also represent single chip memory devices. (*See* B1, B2.)

As discussed above, Bennett discloses ROM chips and implies other chips for reading and writing data, at least suggesting the popular DRAMs for reading and writing. Judge Whyte makes a similar finding:

> Bennett discusses ROMs while explaining the limited number of operations that can be done with a memory device, and it does so to point out that memories like ROMs cannot receive write operations. . . .*Bennett's discussion thus impliedly discloses some type of memory device than can receive write*

[5] *See In re Rambus*, 694 F.3d 42 (Fed.Cir. 2012) (the Federal Circuit holding that the claim term "memory device" in a related Rambus patent includes, but is not limited to, a single chip contrary to Rambus's arguments otherwise).

> *operations. The jury will have to determine at trial whether that implied disclosure encompasses a dynamic random access memory.*

Hynix II at 1137 (emphasis added).

Rambus's allegation that Fujishima's DRAMs would have required other circuitry disclosed in Fujishima to support a cache, Rambus's focus on Bennett's alternative disclosure of separate VBI's and chip substrates, and similar arguments of record, improperly attack the references separately, narrowly constrain the respective teachings, and fail to rebut the Examiner's rationale that Bennett's disclosure of single chip memory substrate devices including VBI's thereon render obvious using well-known DRAM chips as one of such single chip memory devices. (*See, e.g.*, App. Br. 16-18.) Given the genus of memory chips disclosed in Bennett and known to skilled artisans, such skilled artisans would have interpreted Bennett's disclosure as at least suggesting the most popular memory chip: a DRAM.

Rambus maintains that DRAMs were known for high capacity, moderate speeds and low power consumption – instead of fast speed. (*See* App. Br. 17 n. 10.) Contrary to Rambus's arguments, these capacity and power advantages coupled with moderate speed support the obviousness of using a DRAM. Claims 26 and 29 are not limited by any speed constraints or number of pins, and Bennett discloses a versatile system including trivial or simple memory devices – i.e., including memory chips with moderate speeds and relatively few pins, such as three or four. (*See* B4; B8.) According to admissions in the '120 patent, "[t]he number of pins grows with the size of the DRAM" (*see* '120 patent, col. 2, ll. 47-46), and Bennett

similarly indicates a trade-off between the number of pins (which often indicates memory size), complexity, and speed. (*See* Bennett, col. 94, ll. 26-36.) Rambus similarly implies that a single chip could deliver one or more data bits relatively quickly in arguing that chips at the time of the invention had to be aggregated to deliver 16 bits in parallel at relatively higher speeds. (*See* App. Br. 9.)

Contrary to Rambus's related arguments that Fujishima's DRAMs would have been too slow and driven by overly complex systems and thereby would have been unobvious in Bennett's system (*see* App. Br. 13-14), Fujishima discusses as background art a "[c]onventional[] . . . simple cache system . . . utilizing a high-speed access function of a general-purpose DRAM, such as page mode or static column mode" for smaller computer systems at lower cost. (*See* Fujishima, col. 1, ll. 46-52.) Rambus argues that even this 50 ns page mode speed is too slow to use in Bennett's 40 ns system, but Bennett's disclosure is not limited to 40 ns clock cycles, contrary to Rambus's argument (*see* App. Br. 14, n.8) and as the Examiner reasons (*see* AA 8). For example, Bennett states that "the technology is *projected* to drive signals from chip to chip in 20 to 40 nanoseconds" (Bennett, col. 9, ll. 58-60 (emphasis added)) and discloses a variety of memory chips, including relatively fast or large memory devices as indicated *supra* and as discussed further *infra*. As also noted *supra*, higher speeds are harder to obtain as the pin numbers, complexity, and memory size increases. In any event, skilled artisans would have recognized the utility of using a ubiquitous low-cost low power DRAM in place of Bennett's disclosed memory device which includes trivial three-pin simple chips where speed,

cost, memory size, and power are all trade-offs. Claims 26 and 29 read on such a simple memory device and do not require any minimal speed.

In a hearing before the Board on September 12, 2012 involving a related patent (*see* hearing transcript in BPAI 2012-002081 & 2012-001976 (argued together)), Rambus raised a new argument premised on the Federal Circuit's recent decision in *In re Rambus*, *supra* note 5. At the Board hearing, Rambus argued that *In re Rambus* precludes Bennett's interface (the VBI) because it is akin to a complicated processor such as a BIU which the Federal Circuit reasoned was not included in the term "memory device." To the contrary, Bennett's memory device is a slave (B5, B8) and Rambus itself distinguishes masters from slaves, as the Federal Circuit's reasoning points out. *See In re Rambus* at 49-50. *In re Rambus* only precludes as part of a memory device "a global bus controller or CPU, not [the device] from containing a component that interfaces with the computer system, even when that component provides some additional functionality." *Id*. at 50.

In other words, *In re Rambus* does not preclude Bennett's single chip slave devices which merely respond to master bus processor controllers. Bennett also teaches that any device functionality can be disabled to increase speed and distinguishes such "unsophisticated" slave memory devices from "sophisticated" processor master controller devices. (*See* B4, B8.) As such, assuming arguendo Bennett's chip interface has too much control, it would have been obvious to eliminate unneeded functions in the chip interface for the simple single memory chip at issue here. *See In re Sovish*, 769 F.2d 738, 743 (Fed. Cir. 1985) ("This argument presumes stupidity rather than skill.").

Block Value

Rambus maintains that contrary to the Examiner's findings, Bennett does not disclose or suggest the claimed block size information recited in claim 26. (App. Br. 2 (citing Examiner's FOA at 22).) Similar to the single chip issue, *Hynix II* and BPAI 2012-001638 involve Rambus and the block size information issue and essentially agree with the Examiner's findings here.[6]

Rambus's contentions fail to show that the Examiner erred in finding that the claim 26 "block size information" element reads on Bennett's single word read operations. The Examiner, *Hynix II*, and the Board's prior decisions agree that Bennett's single word read operations satisfy the same or similar block size information element.

As one example with regard to the single word read, Bennett states that with respect to the "fast memory" slave device (Bennett, col. 92, l. 33) represented in Figure 32, "[t]he seventh and eight configuration digits establish that 16 data bits will be transferred in 1 Data Cycle" pursuant to a Read (or Write) operation code. (*See* Bennett, col. 92, ll. 33, 42-46; FOA at 22.)[7] Figures 32 and 33 represent similar "fast memory" devices, but Figure 33 employs (4, 4) for the seventh and eight configuration digits, instead of (5, 5), thereby resulting in an 8 bit word over one data cycle which also

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[6] *See Hynix II* at 1125-28, 1139 (discussing Bennett's VII and VIII configuration parameters at issue here). In the Board's '1638 decision at 18, the Board similarly found that Bennett's configuration parameters satisfy a similar claim element set forth in claim 26 of the related Rambus 6,246,916 patent: "block size information . . . representative of an amount of data to be output."

[7] The Examiner relies on Bennett's FUNCTION read code to satisfy the operation code element in claim 26. (*See* FOA 22; B5.)

immediately follows the operation code (i.e., read or write). (*See* Bennett, col.92, l. 15 to col. 94, l. 5; Figs. 32, 33).)

In *Hynix II*, Judge Whyte compared the disclosed block size information parameter in Rambus's related 6,426,916 patent and the recited "block size information" in claim 16 of Rambus's 6,452,863 patent, and concluded that in Bennett, "[i]ndisputably, parameters VII and VIII specify the total amount of data that will be transferred" and that "they . . . specify the total amount of data to be transferred in response to Bennett's basic, single-word read or write operations." *Hynix II* at 1139. Further, referring to the related '916 patent disclosure, Judge Whyte found that *"[a]nalogously*, when Parameter VII equals VIII, the two parameters 'specify' that one data word will be transferred in response to basic read and write operations." *Id*. (emphasis added).

Rambus argues that Bennett's Figures 32 and 36 prove that Bennett does not satisfy the disputed claim term. (App. Br. 3-5.) Rambus reasons that since the two figures transfer different block sizes and employ the same configuration parameters VII and VIII of 5 and 5, this shows that those parameters do not "define[] an amount of data to be output by the memory" as claim 26 requires. (*See* App. Br. 3.)

But the two different results between Figures 32 and 36 only proves that the embodiments are different - as opposed to proving that the configuration parameters do not define the amount of memory output in each embodiment. Bennett refers to two different embodiments by referring to a "large memory" for Figure 36 and a "fast memory" for Figure 32. For example, Bennett refers to Figure 36 as representing a "large memory of up to 2^{32} addresses of 32 bit words." (Bennett, col. 95, ll. 58-59.) On the other

hand, Bennett refers to Figures 31-33 as representing a "fast memory" (Bennett, col. 92, ll. 19-22) in which, for Fig. 32, "the seventh and eighth configuration digits [of (5, 5)] establish that 16 data bits will be transferred in 1 Data Cycle" (*id*. at ll. 44-47 (discussing fast memory configured with parameters 42252**55 –** VII and VIII configuration parameters in bold**.**)).

Rambus does not dispute the Examiner's finding that "Figure 32 deals with 'fast' memory and Figure deals with 'large' memory," but maintains, contrary to the Examiner's rationale, that comparing the two different embodiments is proper because "Bennett makes no distinctions between the operation of the configuration parameters VII and VIII for 'fast' and 'large' memories." (App. Br. 5 (citing Examiner's Advisory Action 6).) This argument fails acknowledge the implicit distinctions by different configuration parameters, result, and nomenclature - *e.g*., "fast" and "large" memory. Moreover, only one embodiment is required to satisfy the claim and Figure 32 satisfies it – as seen by a comparing the resulting block lengths of 16 and 8 bits pursuant to the VII and VIII configuration parameters (5, 5) to (4, 4) shown in fast memory devices represented in Figures 32 and 33.

Figures 32 and 33 represent single word data transfers over a single data cycle pursuant to a Read or Write operation code. As indicated *supra*, for Figure 32, Bennett states that in this fast memory configuration, "[t]he seventh and eighth configuration digits establish that 16 data bits will be transferred in 1 Data Cycle. ." (Bennett, col. 92, ll. 44-46.) "For the Read operation the memory accepts an address provided with a Read operation request and receives and associated data word from the specified address." (Bennett, col. 91, ll. 6-9.) Comparing Figure 32, Bennett states that "[t]he

same Read or Write operation as causes a transaction with a fast memory is shown in FIG. 33 for an alternative 4312244 configuration." (Bennett, col. 93, ll. 56-58.) Consequently, for such a Read, and per Figure 3, the "number of Data Lines is eight, . . . while the number of Data Cycles is one." (Bennett, col. 94, ll. 2-5.)

In other words, Figure 32 (configured as 42252255, col. 92, ll. 47); Figure 33 (configured as 43112244, col. 93, l. 58); and Figure 36 (configured as 4315355, col. 95, l. 49) are configured differently as the configuration digits show. As indicated in the previous paragraph, for a Read or Write operation, the Figure 33 configured species (or sub-species, etc.) transfers an 8 bit block of data over one cycle as dictated by the VII and VIII configuration parameters (4, 4) whereas the Figure 32 configured species transfers a 16 bit block of data over one cycle as dictated by the VII and VIII configuration parameters (5, 5). (*Also compare* Bennett Fig. 33 *with* Fig. 32; *see also* Bennett Fig. 3; *Hynix II* at 1127.) In other words, comparing Figure 32 and Figure 33 shows that Bennett satisfies the disputed claim term since a different combination for the VII and VIII configuration parameters each constitute "block size information [which] define[s] an amount of data to be output by the memory device" as claim 26 requires.

On the other hand, even if Rambus's comparison of Figure 32 to Figure 36 is proper, the comparison must recognize that Figure 36 represents a different "large memory" (Bennett, col. 96, ll. 25-26) case in Bennett which transfers multiple 16 bit words (two data words and two address words) over four successive data cycles. So even though Figure 36 involves transfers of two 16 bit address words over two data cycles followed by two 16 bit data words, the combination of the configuration parameter VII and

VIII values 5 and 5 in that embodiment, "*dictates* that the indicated two sixteen bit addresses will be followed by the indicated two sixteen bit data words" for that particular embodiment. (*See* Bennett, col. 96, ll. 27-29 (emphasis added).) Bennett also refers to Figure 36 as handling "a block of 4 sixteen bit data words." (Col. 96, ll. 41-42.)[8]

In each separate species of Figures 32 and 36, each of which use some of the same parameter values (i.e., 5, 5 for VII and VIII), the separately configured memory devices each dictate what is being transferred. Generally, with respect to single word reads for the fast memory devices, Bennett's system transfers 1, 2, 4, 8, or 16 bit words over one data cycle based on specific configuration parameter VII and VIII values, thereby specifying the claimed block size as set forth in the claim for those single word configurations – i.e., even if Figure 36 presents a special case or otherwise does not satisfy claim 26. (*See* Bennett, Fig. 3.)

That is, the Versatile Bus Interface (VBI) on each configured chip determines how much data to transfer for a single word read and controls the operation based on the configuration; i.e., "'the what (what operations), when (in what relationship and/or sequence)'." (*See* Bennett at col. 39, ll. 31-34).) In an attempt at a distinction, Rambus relies on Bennett's statement that the "'seventh configuration dimension is the format—the partitionment in pins times cycles as equals bits—of data words and is not the amount

[8] Bennett also refers to "32 bit words shown in Fig. 36." (Col. 95, l. 59.) Alternately calling the different groups 16 or 32 bit data (or address) words or a group, etc. shows that the particular nomenclature is not important in Bennett. (*See* note 3 *supra*; Bennett, col. 90, ll. 50-58 (discussing "function" and "data" interchangeably whether pure data, address information, or other operations are transferred over the same multiplexed "data" lines).)

thereof.'" (*See* App. Br. 2 (quoting Bennett at col. 17, ll. 29-31).) Rambus points out that the seventh dimension constitutes a combination of parameters VII and VIII and the Examiner agrees. (App. Br. 2; Ans. 5.) But as the Examiner essentially reasons, the passage only states that generally, the seventh configuration dimension does not specify the total amount of transferred words. (*See* Ans. 5.) On the other hand, for typical single word reads in fast memory systems, the seventh dimension does specify the total amount of data – i.e., since only one word is transferred the configuration parameters specify the total data amount. (*See* Ans. 5-6.) A comparison of Figures 32 and 33 prove this as explained *supra*, and as the District Court finds, "*[i]ndisputably*, parameters VII and VIII *specify the total amount of data that will be transferred* in response to two basic types of transaction requests" - single word reads and writes. *See Hynix II* at 1139 (emphasis added).)

Rambus relies on a similar sentence in the same passage at column 17 of Bennett, i.e., that "block data . . . [can] flow, on the Versatile Bus without . . . *any requirement for or relation to this seventh configuration dimension*." (App. Br. 2 (quoting Bennett at col. 17, ll. 24-29).) But Bennett's statements specifically refer to how the Versatile Bus controls block data transfers, as opposed to what the Versatile Bus Interface on each chip dictates. For example, as indicated *supra*, Bennett states with reference to the large memory represented in Figure 36 that the particularly configured Data Line utilization "*dictates* that the indicated two sixteen bit addresses will be followed by the indicated two sixteen bit data words" for that particular embodiment. (*See* Bennett, col. 96, ll. 27-29 (emphasis added); *see also* col. 95, ll. 1-2.) Bennett also states that the particular "configuration that four

total cycles should be utilized requires naught but some associated control between the Versatile Bus Interface [VBI] Logic(s) and User(s)." (Bennett at col. 96, ll. 33-40.) In other words, Figure 36 involves multiple word transfers and requires "naught but some associated control" with the VBI.

More importantly, Bennett states that the "Versatile *Bus* knows naught . . . . [because t]he Versatile *Bus* is simply handling data." (Bennett, col. 96, ll. 40-41 (emphasis added).) As an example of this control based on the configured parameters and perhaps other associated control, Bennett states that "[i]n FIG. 36 a Versatile Bus of 43153355 configuration has handled a block of 4 sixteen bit data words." (Bennett, col. 96, ll.40-42.)

Even if claim 26 precludes this minimal (i.e., "naught") "associated control," which it does not as discussed further below, in any given memory device contemplated by Bennett wherein such minimal control sets the total number of clock cycles for the block data transfer, the specific Figure 36 configuration ultimately dictates the word length within that configured embodiment, thereby satisfying claim 26. Viewed another way, the Figure 36 species may include different subspecies each of which have different "associated control," for example, to specify 2, 4, or 8 total clock cycles for data transfers, etc., but within each subspecies, the configuration parameters VII and VIII *dictate* the block size. In essence, the associated control and the large physical memory implicit in Figure 36 define it as a "large memory" which handles multiple word data transfers.

This interpretation comports with the '120 patent. In the '120 patent, skilled artisans would have to know which code of several "other block size encoding schemes" will be used to determine the block size for any particular embodiment or device. (*See* '120 patent, col. 11, ll. 59-60.) That

is, the same pattern of bits for different embodiments can represent different block sizes – depending on the encoding scheme. Also, in addition to these other disclosed encoding schemes, even in the preferred embodiment of the '120 patent, the same 3-bit pattern can represent two different block sizes. (*See* '120 patent, col. 11, ll. 39-41 (different first bits dictate the code for the remaining three bits).) In other words, without knowing the particular encoding scheme or first code bit in the '120 patent, skilled artisans could not determine the block size value. For the different encoding schemes envisioned, each particular encoding scheme essentially defines a particular embodiment which governs the block size. Similarly, even if the "associated control" in Bennett helps to define (along with its memory size, pins, etc.) a particular Figure 36 embodiment or subspecies, Figure 36 still satisfies claim 26 because the configuration parameters VII and VIII dictate the block size for each separate combination of VII and VIII for that particular embodiment. And even if the code (5, 5) in Bennett represents a different amount of data for a large memory as compared to a fast memory, it still separately defines the block size for a fast memory and for a large memory – as compared to the code (4, 4), for example, which defines a different amount of data.

Plurality of Input Receivers to Sample Block Size

Rambus states that Bennett does not disclose "input receiver circuitry, including a first plurality of input receivers to sample block size information synchronously with respect to the external clock signal," as claim 26 recites. (App. Br. 5-6.) Rambus acknowledges that the Examiner relies on Bennett's parameters VII and VIII to satisfy the recited block size information features as discussed above, but asserts that

> Bennett's configuration register that includes parameters VII and VIII is set using a Maintenance Processor, which uses a serial interface to shift the various bits to be included in the configuration register . . . Those parameters, which are serially shifted into the VM Node of a User, are not sampled synchronously with respect to an external clock signal by a plurality of input receivers.

(App. Br. 6.)

In the Final Office Action, the Examiner responds to this same argument previously advanced by Rambus and points that out in the Answer. (*See* FOA 9-10; Ans. 9-10 (citing Bennett, col. ll. 46-56).) Rambus's Appeal Brief, which merely repeats Rambus's earlier argument, fails to shed any light on why Rambus deems the Examiner's FOA response to be in error. In summary, the Examiner agrees with Rambus that a maintenance processor in Bennett sends a bit pattern to the configuration register in each memory device, and explains that it sends the bit pattern over several signal lines which the memory device samples synchronously based on the external clock φ2. The Examiner further supports the rejection by relying on other descriptions in Bennett to show that Bennett discloses synchronous communication based on the external clock, a plurality of input/output pins on each memory device, and "DRIVER/RECEIVER logical elements" (Bennett, col. 120, l.35). (*See* Ans. 10-12 (citing Bennett at cols. 81, 120 & 274).) In light of the '120 patent and generic claim 26 "plurality of input receivers" limitation (assuming for the sake of argument Rambus deems that limitation to be missing), each separate input pin in Bennett's memory device corresponds to an input "receiver" (including a logical element)

residing in the memory device, and each chip memory device includes a VBI Node and VBI Logics. (*See* FOA 9-11; Bennett Fig. 1).[9]

In a related proceeding, Rambus identifies Bennett's "three signal lines" as corresponding to these bit lines in Bennett. (*See* Rambus Resp. Br. 8 in Reexamination Control Nos. 95/001,105 & 95/001,133 as discussed further in the BPAI 2012-2081 decision at 25).) The circuitry or logical elements receiving the three signal lines which receive and/or process different bits, reasonably correspond to different (i.e., a plurality) of "receivers" in Bennett's memory device. Rambus does not direct attention as to how the '120 patent defines or limits the "receivers" in claim 26. Moreover, Figure 10 of the '120 patent simply shows black boxes indicating two input receivers (i.e., "INPUT REC") gated by clock complements from one clock and receiving data from what appears to be the same input "PAD" 75. Rambus does not explain why Bennett fails to disclose or render obvious such generic black box DRAM receivers.

The record also indicates the structural features of claim 26, including input "receivers" and output drivers constitute well-known components of typical DRAM memory devices at the time of the invention. For example, the '120 patent describes a "conventional 4 Mbit DRAM" which includes "input and output circuitry connected ultimately to the device pins" and notes that "[m]any of these details have been implemented selectively in certain fast memory devices, but never in conjunction with the bus architecture of this invention." (*See* '120 patent, col. 23, ll. 43-65; Fig. 15.)

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[9] As indicated *supra*, for example, Figure 1 represents the "same VLSIC chip substrate" having a VLSI User (e.g., memory) device, VM node, and VBI logics. (*See* Bennett, col. 24, ll. 21-23; col. 36, ll. 19-25; B1.)

Receiving an External Clock Signal

Rambus argues that Bennett does not disclose a synchronous memory device receiving an external clock signal because "it [i.e., the clock] is only provided to the separate interface . . . the VBI." (App. Br. 18.) This argument constitutes another form of the single chip argument addressed above. Contrary to Rambus's arguments and according to the discussion *supra*, Bennett discloses sending an external synchronous clock signal to its memory devices. (*See also* B6, B7.)

Summary – Claim 26

Based on the foregoing discussion and the discussion below involving secondary considerations, Rambus has not shown that the Examiner erred in rejecting claim 26.

Claim 29

Claim 29 recites the "memory device of claim 26 wherein the input receiver circuitry samples the first operation code synchronously with respect to the external clock signal." Rambus does not argue that Bennett fails to disclose the operation code. (*See supra* note 7 (the Examiner relies on Bennett's single word Read operation code); *see also* Bennett Fig. 34; B5.) Rather, Rambus's argument with respect to claim 29 also constitutes another form of the single chip argument addressed above: "The alleged input receiver circuitry that samples the alleged operation code exists on the VBI, not on the memory chips." (App. Br. 19.) Contrary to Rambus's arguments, based on the foregoing discussion, Bennett discloses sending synchronous clock signals to its memory devices which include the VBI on the same substrate – i.e., on a single chip. (*See* B6, B7 and the discussion *supra*.)

Secondary Considerations

Rambus contends that secondary evidence supports unobviousness. (*See* App. Br. 19-22.) But the evidence fails to establish a nexus because any success likely flows from a variety of several unclaimed features touted here or in other Rambus proceedings or patents as important. Such unclaimed, but disclosed features, include memory controllers, eight data lines, small DRAM sizes with minimal bus loading, multiplexed bus architecture and device interfaces, packetized control, unique device identifiers, time access and arbitration schemes, a 500 MHz data rate, controlled-impedance, double terminated lines, and memory devices having all the functionality of prior art circuit boards. (*See* '120 patent, Abstract, col. 3, ll. 22-47; col. 4, ll. 10-56; col. 7, ll. 10-25; col. 9, ll. 39-65; col. 12, ll. 45-58; col. 14, ll. 48-50; Murphy Decl. ¶¶ 33-37.) *See also Rambus Inc. v. Infineon Technologies AG*, 318 F.3d 1081, 1094-95 (Fed. Cir. 2003) ("The present invention is designed to provide a high speed, multiplexed bus'" (quoting Rambus's related '918 patent, col. 5, ll. 36-46), but "the prosecution history shows that a multiplexing bus is only one of many inventions disclosed in the '898 application.")[10] In other proceedings before the Board, Rambus agrees that "the original disclosure includes many different inventions." (*See* BPAI 2012-002081 decision at 38 (Jan. 19, 2012) (quoting Rambus, citation omitted).) Similarly, Rambus's expert

[10] *See Infineon*, 318 F.3d at 1084-86 (finding that the written descriptions of each of four related Rambus patents, 5,954,804; 5,953,263; 6,034,918; and 6,032,214, are substantially identical to the written description of the 07/510,898 application to which they, and the '120 patent here, all claim continuity).

Murphy stated that "'[t]he original disclosure includes a number of different inventions.'" (*Id*. quoting Murphy Decl. at ¶ 34.)

Rambus's evidence does not demonstrate that any success was due solely to the claimed features here, or to claimed features that were not already known in the prior art. (*See* Ans. 25-30.) Rambus contends "[t]he claimed inventions have also been accepted by the industry, as shown by the numerous licenses to the Farmwald patent family." (App. Br. 21.) But this is a vague statement which lacks a specific nexus to claims 26 and 29 at issue here. Rambus does not provide a copy of any licenses or provide evidence showing what other unclaimed features any of the licenses involve. Also, it is well known and settled law that competitors often take licenses for commercial or other reasons having nothing to do with unobviousness.

Rambus also alleges that "synchronous memory devices have had great commercial success" and that there were other failures in the industry. (*See* App. Br. 21.) But single chip synchronous memory devices were known as Bennett discloses. DRAMs were also known as discussed *supra*. The record suggests that at least part of any commercial success would have been due to the most popular memory chip, a DRAM chip, in general, or, to Bennett's known synchronous chip. *Cf. In re DBC*, 545 F.3d 1373, 1384 (Fed. Cir. 2008) (Board's conclusion of nonobviousness supported, the Board finding, *inter alia*, that "evidence in the record suggested that the success of XanGo™ juice may be due to other factors-for example, the increasing popularity of the mangosteen fruit in general"). The Federal Circuit further reasoned in *DBC* that

> . . . DBC has done little more than submit evidence of sales. However substantial those sales, that evidence does not reveal

> in any way that the driving force behind those sales was the claimed combination of mangosteen fruit, mangosteen rind extract, and fruit or vegetable juice. Nor is there any evidence that sales of XanGo™ juice were not merely attributable to the increasing popularity of mangosteen fruit or the effectiveness of the marketing efforts employed.

Id. at 1384. *See also Ormco Corp. v. Align Technology, Inc*., 463 F.3d 1299, 1312, 1313 (Fed. Cir. 2006) ("[I]f the feature that creates the commercial success was known in the prior art, the success is not pertinent." Also reasoning that success that is due "'partially' to claimed features" and to unclaimed features and/or other features already in the art lacks the requisite nexus to show unobviousness.) (Citations omitted).

While Rambus also argues that the claims solve a memory bottleneck problem and obtain high-speed performance (*see* App. Br. 19-20), claims 26 and 29 read on relatively slow memory devices, since the claims do not recite any speed (as a functional limitation) and do not recite other sufficient and necessary circuitry to obtain such speed.[11] Moreover, Dr. Farmwald testified that "even up into the early part of the '90s, it [speed] wasn't going to be a problem." (*See* Farmwald Trial Dep. 276 (attached as App. Br. Evidence Ex. E-5).) In other words, Dr. Farmwald may have solved a

[11] In another reexamination proceeding, similar to the proceeding here, Rambus alleges "disbelief" and pervasive skepticism "'over a 500 megabit per second DRAM data rate'" and "about many of the specific features of the technology" as showing "'strong evidence of nonobviousness.'" (*See* Rambus Resp. Br. 19 (citations omitted) in the BPAI 2012-000142 reexamination proceeding.) Assuming for the sake of argument that uncorroborated statements by the inventors show skepticism by others, as noted, claims 26 and 29 do not require the 500 MHz speed touted or "many of the other specific features" – whatever they may be.

problem predicted to occur in the future – after the effective filing date of the '120 patent, but not a long-standing problem existing at the time of the invention.

Rambus's allegations of recognition and praise for the "'high bandwidth memory-interface technology'" and bandwidth advances "'as a result of the ideas [Dr. Horowitz] pioneered'" (App. Br. 21 (citation omitted)) point to a lack of nexus as to any success or praise. The devices claimed here have no bandwidth limitation, let alone limitations directed to the myriad other "ideas [Dr. Horowitz] pioneered" – whatever they may have been. For example, the '120 patent states that the high bus bandwidth (high clock rate) is "made possible . . . . [because] [t]he bus lines are controlled-impedance, doubly-terminated lines" and "because of the packaging used." (*See* '120 patent, col. 4, ll. 37-42.) Claims 26 and 29 do not require any of these features or other speed related touted features.

Based on the foregoing discussion, the record suggests that the proffered evidence is not commensurate with the claim scope and lacks a nexus thereto. Rambus has not demonstrated that any success is not due to popular DRAMs in general, synchronous memory chips in general, or, to a whole host of unclaimed features, including the unclaimed but touted multiplexed bus interface, high bandwidth and/or speed, and other unclaimed circuit features, such as the identification feature, arbitration control features, low capacitance and power, precharging circuitry, block data transfer circuitry, and memory controllers. The record indicates that such features (and other pioneering ideas) would have been required to obtain the touted high speed from a single DRAM upon which any alleged

success appears to be based. *See Infineon*, 318 F.3d at 1095 (quoted *supra*, mentioning Rambus's high speed multiplexed system).

CONCLUSION

"For over half a century, the Court has held that a 'patent for a combination which only unites old elements with no change in their respective functions . . . obviously withdraws what already is known into the field of its monopoly and diminishes the resources available to skillful men.'" *KSR Int'l. Co. v. Teleflex Inc.*, 550 U.S. 398, 415-416 (2007) (quoting *Great Atl. & Pac. Tea Co. v. Supermarket Equip. Corp.*, 340 U.S. 147, 152-153 (1950).) Employing a DRAM memory chip device as one of Bennett's memory chip devices "only unites old elements" with no change in function of Bennett's memory chip device and thereby constitutes a "principal reason" for finding the '120 patent claims 26 and 29 obvious. *See KSR*, 550 U.S. at 416. After careful consideration of the record, the obviousness of using a well-known popular DRAM for one of the generic synchronous single chip memory devices in Bennett outweighs the proffer of secondary considerations.

AFFIRMED

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