



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/259,791	10/27/2005	Mark Suska	20663US02	6695
23446	7590	02/01/2013	EXAMINER	
MCANDREWS HELD & MALLOY, L.L.P. 500 WEST MADISON STREET SUITE 3400 CHICAGO, IL 60661			DIEP, TRUNG T	
			ART UNIT	PAPER NUMBER
			2664	
			NOTIFICATION DATE	DELIVERY MODE
			02/01/2013	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

mhmpto@mcandrews-ip.com

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte MARK SUSKA

Appeal 2012-008105
Application 11/259,791
Technology Center 2600

Before THU A. DANG, JAMES R. HUGHES,
and GREGORY J. GONSALVES, *Administrative Patent Judges*.

DANG, *Administrative Patent Judge*.

DECISION ON APPEAL

I. STATEMENT OF THE CASE

Appellant appeals under 35 U.S.C. § 134(a) from a Final Rejection of claims 24-26 and 28-59 (App. Br. 4). Claims 1-23 and 27 have been canceled (App. Br. 25). We have jurisdiction under 35 U.S.C. § 6(b).

We affirm-in-part.

A. INVENTION

Appellant's invention is directed to an imaging array sensor having an interface that stores data and clocking signals to liberate space within a microprocessor coupled thereto; wherein, the interface includes a circuit that controls the transfer of data from the memory within the interface to the microprocessor (Abstract; Spec. 7:1-6).

B. ILLUSTRATIVE CLAIM

Claim 24 is exemplary:

24. A system, comprising

an imaging array of sensing pixels configured to generate imaging data; and

a buffer configured to store the imaging data received at an input port, store clocking signals at a rate determined by the clocking signals, and output the imaging data through an output port to a data bus.

C. REJECTIONS

The prior art relied upon by the Examiner in rejecting the claims on appeal is:

Booth, Jr	U.S. 6,947,085 B1	Sep. 20, 2005
Yamada	JP 09298714 A	Nov.-1997

Claim 24 stands rejected under 35 U.S.C. § 102(b) as being anticipated by Yamada.

Claims 28-30, 36-39, 41-43, 45, 49-52, 54-56, and 58 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Booth.

Claims 24-26, 31-35, 44, 46-48, 53, and 59 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Booth in view of Yamada.

Claim 57 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Booth.

II. ISSUES

The dispositive issues before us are whether the Examiner has erred in determining that:

1. Yamada discloses “a buffer *configured to* store the imaging data received at an input port, store clocking signals at a rate determined by the clocking signals, and output the imaging data through an output port to a data bus” (claim 24, emphasis added);

2. Booth discloses “a signal generator *configured to* seek control of the data bus if the quantity of data in the memory attains a predetermined level” and “a circuit *configured to* respond to the availability of the data bus and to control transfer of the stored data through the output port” (claim 28, emphasis added);

3. Booth discloses “generating a request to transfer image data from the memory in response to a predetermined amount of data being stored in the memory; and *transferring image data from the memory in response to the request*” (claim 36, emphasis added); and

4. Booth discloses “a counter *configured to* determine *the quantity of imaging data in the buffer*” (claim 49, emphasis added).

III. FINDINGS OF FACT

The following Findings of Fact (FF) are shown by a preponderance of the evidence.

Yamada

1. Yamada discloses a still camera having an image pickup device 102 that sends Red-Green-Blue (RGB) color signals data to a First-In-First-Out (FIFO) memory cell 120 (within a FIFO register 116) which transmits the RGB data to a microprocessor 106 at an output port of the FIFO register 116 (¶ [0030]-[0031]).

2. A write-in address register 122 within the FIFO register 116 receives at its input port clocking signals (write-in clock signal W_{CLK} and write-in reset signal W_{RST}) and generates a write-in address $ADRW$ at its output port; wherein, the write address register 122 is formed in the storage area of the FIFO116 (¶ [0032]).

Booth

3. Booth discloses an image sensor 10 coupled to an interface control 32 including a memory 36 and two counters (a write counter 37 and a read counter 38) which indicate the data count stored (read) in memory 36 and the data count read out of memory to a data processing circuit 63; wherein, a data overload sensor 33 determines whether the storage buffer of memory 36 is full using a comparing circuit 39 that compares the counts of counters 37 and 38 (Figs. 3a, 3b, and 6; col. 3, ll. 33-67).

4. When the data overload sensor 33 detects data overflow, it generates a flow control signal 35 that is sent to the image sensor 10 to halt the transmission of the video signals (Figs. 3b and 6; col. 3, ll. 43-45).

IV. ANALYSIS

Claim 24

Appellant contends that “Yamada never mentions that the FIFO memory 116, write-in address register 122, or the read-out address register 124 is implemented as a serial-in to serial-out shift register” (App. Br. 13). Appellant argues further that “Yamada never discloses storing either of these two clock signals;” “[i]nstead, Yamada discloses storing R, G, and B data in memory cell 120 and reading R, G, and B data from memory cell 120” (App. Br. 14-15).

However, the Examiner finds that “an electronic camera including a first-in first out (FIFO) memory 116 that contains the write-in address register 122 and the read-out address register 124, the write-in address register 122 for temporarily storing the write-in clock signal W_{CLK} and write-in reset signal W_{RST} within the memory” and “[t]he write-in address register 122 generates write address ADRW which serves as a write-in timing and/or clock signal for storing the pixel data, transmitted from microprocessor 106, into the memory cell 120” (Ans. 21). Thus, “Yamada’s teaching clearly encompasses the claimed limitation as to ‘a buffer configured to store clocking signals’” (*id.*). (Italics omitted.)

Appellant’s argument that “FIFO memory 116 ...[is] implemented as a serial-in to serial-out shift register” (App. Br. 13) is not commensurate in scope with the specific language of claim 24. In particular, claim 24 does not recite such “serial-in to serial-out shift register” as Appellant argues.

We give the claim its broadest reasonable interpretation consistent with the Specification. *See In re Morris*, 127 F.3d 1048, 1054 (Fed. Cir.

1997). Since claim 24 does not define a “buffer,” we give “buffer” its broadest interpretation as a storage register.

Further, claim 24 merely requires that the buffer is “configured to” store the imaging data and clocking signals and to output the imaging data through an output port to a data bus. We find such “configured to” language to merely represent a statement of intended function of the buffer. An intended function will not limit the scope of the claim because it merely defines a context in which the invention operates. *Boehringer Ingelheim Vetmedica, Inc. v. Schering-Plough Corp.*, 320 F.3d 1339, 1345 (Fed. Cir. 2003). Thus, we conclude that claim 24 merely requires that the buffer is capable of performing such intended functions.

Furthermore, we note that “imaging data” and “clocking signals” merely comprise the type of data that is being stored and output by the interface but does not change the functionality of or provide an additional function to the interface. That is, what type of data is being stored and output does not change or limit how the interface stores or outputs the data. Rather, this term is merely a description of the type of data used for comparing.

When descriptive material is not functionally related to the claimed medium, the descriptive material will not distinguish the invention from the prior art in terms of patentability. *See In re Ngai*, 367 F.3d 1336, 1339 (Fed. Cir. 2004) and *In re Gulack*, 703 F.2d 1381, 1385 (Fed. Cir. 1983).

Accordingly, we give “a buffer configured to store the imaging data received at an input port, store clocking signals at a rate determined by the clocking signals, and output the imaging data through an output port to a data bus” its broadest reasonable interpretation as any register that is capable

of storing and outputting data, as consistent with the Specification and claim 24.

Yamada discloses a still camera having an image pickup device that generates and sends RGB (image) data to a FIFO memory cell within a FIFO register which transmits the RGB data to a microprocessor (FF 1). The FIFO register also includes a write-in address register formed within its storage area; wherein, the write-in address register receives at its input port a write-in clock signal and a write-in reset signal (FF 2). We find that FIFO to be a register that is capable of storing imaging data and clocking signals and outputting the imaging data.

Accordingly, we find that Appellant has not shown that the Examiner erred in rejecting claim 24 under 35 U.S.C. § 102(b) over Yamada.

Claim 28-30 and 58

Appellant contends that “Booth does not disclose ‘a signal generator configured to seek control of a data bus,’” “[i]nstead, Booth discloses that a data overload sensor 33 sends a flow control signal 35 to the image sensor 10 to halt the transmission of video signals” (App. Br. 16). Appellant argues that “the interface control 32 does not ‘respond to the availability of the data bus’ between the buffer memory 36 and the data processing circuitry 63 in order ‘to control transfer of the stored data through the output port’ to the data processing circuitry 63” (App. Br. 17).

However, the Examiner finds that Booth discloses “the comparing circuit 39 and the data overload sensor 33, in combination, functions as the signal generator which is to detect data overflow from sense line 34, to generates a flow control signal 35 to be sent to the image sensor 10 to halt the transmission of the video signal” and the “[a]mount of data in the buffer

memory is detected as ‘the buffer memory is full’ can be equated to ‘the quantity of data in the memory attains a predetermined level’” (Ans. 22). The Examiner finds further that “the interface control 32 functions as a circuit for managing the data arriving and leaving the interface control 32” which “is to be further processed by data processing circuitry 63” (Ans. 22-23).

Appellant’s argument that “the interface control 32 does not ‘respond to the availability of the data bus’ between the buffer memory 36 and the data processing circuitry 63 in order ‘to control transfer of the stored data through the output port’ to the data processing circuitry 63” (App. Br. 17) is not commensurate in scope with the specific language of claim 28. In particular, claim 28 does not recite such “availability of the data bus *between the buffer memory and the data processing circuitry*” or “*in order to control transfer of the stored data through the output port*” as Appellant argues.

Claim 28 merely requires that the signal generator is “configured to” seek control of the data bus when the data within memory reaches a predetermined level and that the circuit is “configured to” respond to the availability of the data bus and control data transfer. We give “a signal generator configured to seek control of the data bus if the quantity of data in the memory attains a predetermined level” its broadest reasonable interpretation as a circuit that generates signals which is *capable of* seeking control of the data bus when the data in memory reaches a predetermined level, as consistent with the Specification and claim 1. We also give “a circuit configured to respond to the availability of the data bus and to control transfer of the stored data through the output port” its broadest reasonable interpretation as a circuit capable of using the data bus when available and

controlling the transfer of stored data, as consistent with the Specification and claim 28.

Booth discloses an image sensor coupled to an interface control and a data overload sensor that determines whether the storage buffer of memory within the interface control is full (a predetermined level of data); wherein, the data overload sensor generates a flow control signal to be sent to the image sensor when the storage buffer is full to halt the transmission of data (FF 3 and 4). We find that data overload sensor represents a signal generator that is capable of seeking control of the data bus when the quantity of data in memory attains to a predetermined level. We find further that the interface control is capable of using the data bus when available and controlling the transfer of the stored data through the output port.

Accordingly, we find that Appellant has not shown that the Examiner erred in rejecting claim 28 under 35 U.S.C. § 102(e) over Booth. Further, claims 29, 30, and 58 (depending from claim 28) which have not been argued separately, fall with claim 28.

Claim 36-39, 41-43, and 45

Appellant contends that “even if Booth discloses generating a flow control signal ‘in response to a predetermined amount of data being stored in the memory’ 36 ... , such a flow control signal requests the image sensor 10 to stop transmitting data to the memory 36; it does not request that image data be transferred from the memory 36” (App. Br. 19).

After reviewing the record on appeal, we agree with Appellant. Though we agree with the Examiner that Booth does disclose a data overload sensor that determines whether the storage buffer of memory within the interface control is at a predetermined amount of data (full);

wherein, the data overload sensor generates a flow control signal to be sent to the image sensor (FF 4), we cannot find any teaching in the Examiner's recited portion of Booth that "generating a request *to transfer image data from the memory* in response to a predetermined amount of data being stored in the memory; and transferring image data from the memory *in response to the request*" as required by claim 36 (emphasis, added) in the recited portions of Booth referenced by the Examiner. That is, although the data overload sensor generates a flow control signal in response to a predetermined amount of data stored in memory, this flow control signal *does not request that data be transferred from memory in response to a predetermined amount of data being stored in memory*; rather, it instructs the image sensor to halt the transfer of data from the image sensor to the interface control.

Accordingly, we find that Appellant has shown that the Examiner erred in rejecting claim 36 under 35 U.S.C. § 102(e) over Booth. Further, claims 37-39, 41-43, and 45 (depending from claims 36) stand with claim 36.

Claims 49-52 and 54-56

As to independent claim 49, Appellant contends that although Booth discloses that "the write counter 37 maintains a count and the read counter 38 maintains a count, but neither of these counts are a quantity of imaging data in the memory 36" (App. Br. 20). In particular, Appellant argues that the comparing circuit "in making such [a] determination [of the memory being full] ... does not necessarily determine the quantity of data in the memory, but merely a condition of the memory 36" (*id.*).

However, the Examiner finds that Booth discloses that “the data overload sensor senses the full buffer memory through a comparing circuit” (Ans.25). Thus, “*Booth’s teaching clearly encompasses the claimed limitation as to determine the quantity of data in the memory and/or buffer*” (*id.*).

Claim 49 merely requires that the counter is “configured to” determine the quantity of imaging data in the buffer. We give “a counter configured to determine the quantity of imaging data in the buffer” its broadest reasonable interpretation as a counter that is *capable of* determining the quantity of imaging data in the buffer, as consistent with the Specification and claim 49.

As noted *supra*, Booth discloses an interface control having a memory coupled to a write counter and a read counter which indicate the data count read in and out of memory (FF 3). The interface control also includes a comparing circuit that compares the counts of the write and read counters to determine whether the memory is full (*id.*). We find that the write and read counters coupled to the comparing circuit represent a counter that is capable of determining the quantity of the imaging data stored in the memory. That is, we find that Booth’s write and read counters coupled to the comparing circuit comprises “a counter configured to determine the quantity of imaging data in the buffer” (claim 49).

Accordingly, we find that Appellant has not shown that the Examiner erred in rejecting claim 49 under 35 U.S.C. § 102(e) over Booth. Appellant provides a similar argument for independent claim 54 which includes similar claim language. Therefore, independent claim 54 having similar claim

limitations and claims 50-52, 55, and 56 (depending from claims 49 and 54) which have not been argued separately, fall with claim 49.

Claims 24-26, 31-35, 37, 44, 46, 48, 53, and 59

Appellant argues that claims 24-26, 31-35, 37, 44, 46, 48, 53, and 59 is patentable over the cited prior art for the same reasons asserted with respect to claim 24 (App. Br. 22).

As noted *supra*, however, we find that Yamada teaches all the features of claim 24. We therefore affirm the Examiner's rejection of claims 24-26, 31-35, 37, 44, 46, 48, 53, and 59 under 35 U.S.C. § 103 over Booth in view of Yamada for the same reasons expressed with respect to claim 24, *supra*.

Claim 47

Appellant argues that claim 47 is patentable over the cited prior art for the same reasons asserted with respect to claim 24 and "Yamada does not teach that the write-in register 122 is configured to output the write-in address ADRW through the output port of the memory 120" (App. Br. 23). However, the Examiner notes that he has relied upon the combined teachings of Booth and Yamada (Ans. 29-30).

Claim 47 merely requires that the buffer is "configured to" output clocking signals through its output port to a data bus. We give "the buffer is further configured to output the clocking signals through the output port to the data bus" its broadest reasonable interpretation as a buffer that is *capable of* outputting clocking signals, as consistent with the Specification and claim 47.

As noted *supra*, Yamada discloses a FIFO register that couples to receive a write-in clock signal and a write-in reset signal and couples to a microprocessor at its output port (FF 2). We find that the FIFO register

comprises a buffer the couples to receive clocking signals at its input port and is capable of outputting these same clocking signals at its output port. In particular, we find that Yamada's FIFO register comprises a "buffer [that] is further configured to output the clocking signals through the output port to the data bus" (claim 47).

Accordingly, we find that Appellant has not shown that the Examiner erred in rejecting representative claim 47 under 35 U.S.C. § 103(a) over Booth in view of Yamada.

Claim 57

We affirm *supra* the rejection of parent claim 28 under 35 U.S.C. §102 as anticipated by Booth. Appellant presents no separate argument for the patentability of dependent claim 57. We therefore affirm the rejection of claim 57 under 35 U.S.C. § 103 as over Booth for the same reasons expressed with respect to parent claim 28, *supra*.

V. CONCLUSION AND DECISION

The Examiner's rejection of claim 24 under 35 U.S.C. § 102(b), of claims 28-30, 49-52, 54-56, and 58 under 35 U.S.C. § 102(e), and of claims 24-26, 31-35, 44, 46-48, 53, 57, and 59 under 35 U.S.C. § 103(a) is affirmed. The Examiner's rejection of claims 36-39, 41-43, and 45 under 35 U.S.C. § 102(e) is reversed

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED-IN-PART

Vsh