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STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C. 1100 NEW YORK AVENUE, N.W. WASHINGTON, DC 20005			CHOI, WOO H	
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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

NVIDIA CORPORATION
Respondent, Requester

v.

RAMBUS, INC.
Patent Owner, Appellant

Appeal 2012-003817
Inter partes Reexamination Control No. 95/001,205
Patent 7,360,050
Technology Center 3900

Before HOWARD B. BLANKENSHIP, KARL D. EASTHOM, and
STEPHEN C. SIU, *Administrative Patent Judges*.

SIU, *Administrative Patent Judge*.

DECISION ON REQUEST FOR REHEARING

In papers filed October 11, 2012, Appellant requests a rehearing under 37 C.F.R. § 41.79 from the Decision of the Patent Trial and Appeal Board (hereinafter Board), dated November 16, 2012. In the Opinion, we affirmed

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the Examiner's rejection of claims 1, 3, and 7-10 as anticipated by Ware; claims 1-3, 5-20, 22, 23, 25, 26, and 28-31 as unpatentable over Ware and Gustavson; claims 2, 5, 6, 11-14, 16, 17, 19, 20, 22, 23, 25, 26, and 28-31 as unpatentable over Ware and Ohshima; claims 1, 3, 7-11, and 15-18 as unpatentable over Ware and JEDEC; claims 2, 5, 6, 12-14, 19, 20, 23, 25, 26, and 28-31 as unpatentable over Ware, JEDEC, and Gustavson; and claims 2, 5, 6, 19, 20, 23, 26, 28, 29, and 31 as unpatentable over Ware, JEDEC, and Gustavson.

Appellant argues that “[t]he independent claims . . . are clear with respect to ‘write command’ originating outside of the claimed integrated circuit memory device, and being provided to or received by the integrated circuit memory device” and that Ware fails to disclose Start R/W as having an “external origin” (Req. Reh’g. 5). However, Appellant does not specifically indicate which independent claim requires that the “write command” originates outside of an integrated circuit memory device or any specific location from which the write command must originate. Claim 1, for example, recites a write command that specifies that the memory device receive write data and store the write data but does not appear to recite that the write command must originate from any specific location, much less from an “external” location. We are therefore not persuaded by Appellant’s argument.

Even assuming that at least one disputed claim required that the write command originate externally, we note that Ware provides this disclosure

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(*see, e.g.*, Fig. 17 showing Start R/W originating from outside – *i.e.*, external to – the DRAM control logic 500).

Appellant argues that “Ware does not disclose that its Start R/W signal is ‘provided to’ or ‘received’ by the . . . memory device” (Req. Reh’g 5). We disagree with Appellant for at least the reasons previously set forth in the Opinion. For example, Ware discloses Start R/W being “provided to” the DRAM control logic (*see, e.g.*, Fig. 17 illustrating Start R/W being “provided to” DRAM control logic 500). Appellant does not indicate how a write sequence can be initiated by memory as disclosed by Ware without receiving the signal that initiates the write sequence. We disagree with Appellant that the memory of Ware writes data (*i.e.*, the write sequence being “initiated”) without receiving an instruction to do so (*i.e.*, Start R/W) – or being provided with the instruction – that is disclosed as initiating the write sequence in the first place.

Appellant argues that “[t]he Board overlooked the fact that Ware itself distinguishes its ‘write command’ from its ‘Start R/W’ timing signal” (Req. Reh’g 9) and that “Ware does not use the terms ‘write command’ and ‘Start R/W’ interchangeably” (Req. Reh’g 10). Thus, it appears that Appellant argues that the “write command” as claimed differs from “Start R/W” of Ware because, according to Appellant’s implication, Ware does not explicitly disclose that the “Start R/W” is a “write command.” We disagree with Appellant for at least the reasons previously stated in the Opinion.

Claim 1, for example, recites that the write command specifies that a memory device receive write data and store the write data at a location. One of ordinary skill in the art would have understood that specifying a memory device to receive write data and storing the write data at a particular location is merely a write operation in which data is written (and stored) at a particular location. As previously discussed in the Opinion, Ware discloses that “Start R/W” initiates a write sequence (*see, e.g.*, Fig. 17). One of skill in the art would have understood a “write sequence” to include a write operation in which data is written (and stored) to a specific desired location in memory. Since the “write command” as claimed performs this same function (*i.e.*, writing data to a specified location of a specified memory device), we continue to discern no difference between the write command as claimed and Ware’s disclosure.

Appellant argues that Ware fails to disclose the “dual functionality of the . . . ‘write command’” (Req. Reh’g 11) as claimed because, according to Appellant, Ware “does not convey the information as to what operation is to be performed” by Start R/W (Req. Reh’g 11). We disagree with Appellant for at least the reasons previously provided in the Opinion. Contrary to Appellant’s assertion that Ware fails to disclose what operation Start R/W initiates, Ware actually discloses that Start R/W initiates a “write sequence” (*see, e.g.*, Fig. 17), which Appellant does not differentiate from the write operation that is initiated by the “write command” as recited in the disputed claims.

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We have considered Appellant's arguments but find no points that we have misapprehended or overlooked. Therefore, the Request for Rehearing is DENIED.

DENIED

alw

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