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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

NVIDIA CORPORATION
Respondent, Requester

v.

RAMBUS, INC.
Patent Owner, Appellant

Appeal 2012-003816
Inter partes Reexamination Control No. 95/001,196
Patent 7,330,952
Technology Center 3900

Before HOWARD B. BLANKENSHIP, KARL D. EASTHOM, and
STEPHEN C. SIU, *Administrative Patent Judges*.

SIU, *Administrative Patent Judge*.

DECISION ON REQUEST FOR REHEARING

In papers filed October 11, 2012, Appellant requests a rehearing under 37 C.F.R. § 41.52 from the Decision of the Patent Trial and Appeal Board (hereinafter Board), dated September 12, 2012. In the Opinion, we affirmed

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the Examiner's rejection of claims 13, 15-17, and 26 as anticipated by Ware; claims 5, 7-9, 11, 18, 19, 21, 22, 24, 25, and 27 as unpatentable over Ware and Gustavson; and claims 5, 7-9, 11, 18, 19, 21, 22, 25, and 27 as unpatentable over Ware and Ohshima.

Appellant argues that the Board misapprehended the construction of the term “‘write command’ as ‘any instruction or data element that specifies that a device receive write data’ (Req. Reh’g 3) but that “this construction does not impact the basis for this rehearing” (Req. Reh’g 4). Appellant does not provide an alternate construction of the term “write command” or evidence demonstrating a difference between a “write command” and our previously stated broad but reasonable construction of the term.

Appellant argues that a “write command” is “transmitted over [its] own ‘control’ bus from the memory controller,” thus implying that a “data element” is not transmitted over its own control bus from a memory controller. However, Appellant does not provide sufficient evidence to demonstrate that a “write command” must be transmitted over its own control bus or that a “data element” cannot be transmitted over its own control bus. We therefore continue to disagree with Appellant’s contention that we misapprehended the construction of the term “write command” for at least the reasons previously provided (*see, e.g.,* Opinion 6-7).

Appellant argues that “the Board’s broad construction is at odds with [the] Examiner’s . . . construction” of the term (Req. Reh’g 11). We disagree with Appellant at least because the Examiner (as observed by

Appellant) does not provide a definition of the term “write command” (*see, e.g.,* Appellant’s observation that “[t]he Examiner did not explicitly construe the term ‘write command’” – Req. Reh’g. 11). More importantly, Appellant does not demonstrate that “Start R/W” of Ware differs in any way from the “write command” as recited in the disputed claim (*i.e.,* a write command that specifies that a memory device receive write data and store the write data in memory cells, as recited in claim 21, for example).

Appellant alleges that the Board “overlooked the fact that Ware’s Start R/W timing signal does not specify ‘that a device receive write data’ [which is] reserved for Ware’s write command, not its Start R/W timing signal” (Req. Reh’g 3). We disagree with Appellant for at least the reasons previously stated (*see, e.g.,* Opinion 7). For example, Ware discloses a write command (col. 8, l. 53) and an exemplary structure in which a “Start R/W” instruction initiates an operation (*i.e.,* a “write sequence” – *see* Fig. 17) that one of skill in the art would have understood to be a write operation since both the “Start R/W” of Ware and the write command result in the performance of a write operation (or “sequence”).

Appellant alleges that the Board “overlooked the fact that Ware does not disclose the origin of its Start R/W signal . . . [because] Ware does not disclose that its Start R/W signal is ‘provided to’ or ‘received’ . . . by the memory device” (Req. Reh’g 3). We disagree with Appellant at least for the reasons previously stated (*see, e.g.,* Opinion 6-8). For example, Ware discloses a dynamic random access memory (DRAM) (*see, e.g.,* col. 1, ll. 9-

11) that receives a write command (*see, e.g., col. 8, l. 53*) with a programmable write latency (*see, e.g., col. 8, l. 60*) by delaying the signal (*e.g., the “Start R/W”*) in the DRAM control logic (*see, e.g., col. 8, ll. 62-65*). In other words, Ware discloses a Start R/W signal displaying a programmable write latency that is delayed via DRAM control logic. Claim 5, for example, recites a write command that specifies that the memory device receive write data and store the write data in the memory. Since the Start R/W signal of Ware initiates a write sequence (*see, e.g., Fig. 17*) and one of skill in the art would have understood that initiating a write sequence includes initiating a process that writes data into memory (a “write sequence” being a sequence of steps that result in writing data into memory), Ware discloses that the Start R/W signal of Ware specifies a memory device to receive write data and store the write data in the memory, as recited in claim 5, for example.

While Appellant now argues that Ware fails to disclose that the Start R/W signal is “provided to” or “received by” a memory device, Appellant does not indicate how a write sequence can be initiated by memory as disclosed by Ware without receiving the signal that initiates the write sequence. We disagree with Appellant that the memory of Ware writes data (*i.e., the write sequence being “initiated”*) without receiving an instruction to do so (*i.e., Start R/W*) – or being provided with the instruction – that is disclosed as initiating the write sequence in the first place.

Appellant argues that Ware fails to disclose that the write command “is provided to the memory device from an external source” (Req. Reh’g 6). Appellant does not indicate that any of the disputed claims recite that the write command is received “from an external source.” While Appellant cites claims 21 and 26 (Req. Reh’g 6), Appellant does not indicate that either claim 21 or claim 26 recites that the write command is received “from an external source.” At least because none of the disputed claims appear to require that the write command be received “from an external source,” we are not persuaded by Appellant that Ware’s alleged lack of disclosure of this feature is pertinent.

In any event, even assuming that claim 21 or 26 recited that the write command is received “from an external source,” we are still not persuaded by Appellant that Ware fails to disclose this feature. As illustrated in Fig. 17 of Ware, the Start R/W signal is received from a control line 505 external to the DRAM control logic (component 500) (*see, e.g.*, Fig. 17 that illustrates the Start R/W being received from outside – *i.e.*, “external” to – the DRAM control logic 500).

Appellant alleges that the Board “overlooked the fact that Ware never conflates its disclosure of a ‘write command’ with its single bit “Start R/W” timing signal, which is separately and distinctly identified as ‘a signals to initiate an operation’” (Req. Reh’g 3). However, as explained in the Opinion, we disagree with Appellant that Ware fails to disclose the “write command” as recited in the disputed claims (*see, e.g.*, Opinion 6-8).

Claim 5, for example, recites a write command that specifies a memory device receive write data and store the write data in the memory during a write operation while Ware discloses a Start R/W signal that initiates a write sequence (*see, e.g.*, Fig. 17) and one of skill in the art would have understood that a write sequence (as initiated by the Start R/W in Ware) would specify a memory device to write and store data in memory during a write operation, as recited in claim 5, for example.

Appellant argues that the Start R/W signal of Ware “is a single-bit, timing signal that . . . only ‘initiates an operation’” (Req. Reh’g 4) that “does not even specify what operation will be initiated” (*id.*). Thus, Appellant argues that Ware’s Start R/W signal cannot be the claimed “write command” because Ware does not disclose what operation the Start R/W signal initiates. We disagree with Appellant. Contrary to Appellant’s assertion that Ware fails to disclose what operation the Start R/W signal initiates, Ware actually discloses that the Start R/W initiates a “write sequence” (*see, e.g.*, Fig. 17), which Appellant does not differentiate from the write operation that is initiated by the “write command” as recited in the disputed claims.

Appellant argues that while Ware discloses that the Start R/W initiates a write sequence, Ware nevertheless fails to disclose the Start R/W specifying that a device receive data. However, one of skill in the art would have understood that data is written to a device during a write sequence and that a device would have to be specified as the device into which the data is

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to be written in order for the write operation or sequence to be performed.
Appellant does not adequately explain how a device is not specified as receiving data in a write sequence (initiated by a Start R/W signal) in which data is written to a device.

We have considered Appellant's arguments but find no points that we have misapprehended or overlooked. Therefore, the Request for Rehearing is DENIED.

DENIED

alw

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