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Robert D. Shedd, Patent Operations THOMSON Licensing LLC 2 Independence Way Suite 200 Princeton, NJ 08540-6620			TRAN, TRANG U	
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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte DAVID GLEN WHITE and MATTHEW THOMAS MAYER

Appeal 2012-000116
Application 11/525,300
Technology Center 2400

Before THU A. DANG, JAMES R. HUGHES, and
GREGORY J. GONSALVES, *Administrative Patent Judges*.

GONSALVES, Administrative Patent Judge

DECISION ON APPEAL

STATEMENT OF THE CASE

Appellants appeal under 35 U.S.C. § 134(a) from the rejection of claims 1-4 (App. Br. 2). Claims 6-11 were cancelled (*id.*). Claim 5 was objected to (*id.*). We have jurisdiction under 35 U.S.C. § 6(b).

We affirm.

The Invention

Exemplary claim 1 follows:

1. An apparatus for isolating a noise intolerant device from a source of noise, comprising:

a processor for producing clock and data signals and a control signal; and

a digital bus that couples said clock and data signals and said control signal to a buffer,

where, in response to said control signal, said buffer selectively couples said clock and data signals to respective clock and data inputs of said noise intolerant device such that said noise intolerant device is operatively coupled to said processor via said digital bus only when said processor is communicating with said noise intolerant device.

Claims 1-5 stand rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 1 of White (U.S. Patent No. 7,164,449 B1) (Ans. 4).

Claim 1 stands rejected under 35 U.S.C. § 102(b) as being anticipated by Akira (JP Publication No. 60144857 A) (Ans. 4-5).

Claims 2-4 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Akira in view of Tults (U.S. Patent No. 6,693,678 B1).

ISSUE

Appellants' responses to the Examiner's positions present the following issue:

Does Akira disclose that:

in response to said control signal, said buffer selectively couples said clock and data signals to respective clock and data inputs of said noise intolerant device such that said noise intolerant device is operatively coupled to said processor via said digital bus only when said processor is communicating with said noise intolerant device

as recited in independent claim 1?

ANALYSIS

Anticipation Rejection of Claim 1

Appellants contend that the Examiner erred in rejecting independent claim 1 as being anticipated because Akira's system is not capable of performing the claim limitations emphasized above (App. Br. 4-7). In support of their contention, Appellants argue that "when the CPU 2 is not accessing either memory 3 or 4 and is not communicating with the peripheral element 8, the peripheral element 8 is still coupled to the CPU 2" (*id.* at 5).

We agree with Appellants. In Akira, when the CPU 2 is not accessing either memory 3 or 4, the output of the NOR gate of circuit 14 is at logic one (Akira, FIG. 2). As a result, the buffer enabling signal at the output of the OR gate in circuit 14 is at logic one, thereby causing the buffer 1 to couple the peripheral element 8 to the CPU 2 regardless of the value of the peripheral access signal 12 (*id.*). In other words, contrary to the requirement of claim 1, the peripheral element 8 is coupled to the CPU 2 even when they

are not communicating. Accordingly, we find error in the Examiner's anticipation rejection of claim 1.

Obviousness Rejection of Claims 2-4

We also find error in the Examiner's obviousness rejection of claims 2-4 dependent from claim 1 over Akira and Tults because the Examiner did not assert that Tults teaches the claim limitation that is missing from Akira (*see* Ans. 5-7).

Obviousness-Type Double Patenting Rejection of Claims 1-5

We sustain the Examiner's nonstatutory obviousness-type double patenting rejection of claims 1-5 pro forma because Appellants did not set forth any argument relating to these rejections (*see* App. Br. 4-9).

DECISION

We reverse the Examiner's decision rejecting claim 1 as being anticipated under 35 U.S.C. § 102(b) and claims 2-4 as unpatentable under 35 U.S.C. § 103(a).

We affirm the Examiner's rejection of claims 1-5 on the ground of nonstatutory obviousness-type double patenting.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED

llw