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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte MENG DING, AMOL RAMESH JOSHI, LEI XUE, TAKASHI
ORIMOTO, and KUO-TUNG CHANG

Appeal 2011-002776
Application 11/458,046
Technology Center 2800

Before CARL W. WHITEHEAD, JR., ERIC S. FRAHM, and ANDREW J.
DILLON, *Administrative Patent Judges*.

FRAHM, *Administrative Patent Judge*.

DECISION ON APPEAL

STATEMENT OF CASE

Introduction

Appellants appeal under 35 U.S.C. § 134(a) from a final rejection of claims 1-10. Claims 11-20 have been canceled. We have jurisdiction under 35 U.S.C. § 6(b). We reverse.

Exemplary Claim

Exemplary independent claims 1 and 6 under appeal, with emphases added, read as follows:

Claim 1: A memory cell manufacturing method comprising:
forming a first insulator layer over a semiconductor substrate;
forming a charge trap layer over the first insulator layer;
forming an intermediate layer over the charge trap layer; and
forming a second insulator layer from an upper portion of the intermediate layer;
wherein the charge trap layer comprises a first material and the intermediate layer comprises a second material, wherein the first material is situated adjacent to the first insulator layer and the second material is situated adjacent to the second insulator layer *so as to cause a charge-storage bi-layer formed by the charge trap layer and the intermediate layer to have increased data retention.*

Claim 6: A memory cell manufacturing method comprising:
forming a first dielectric layer over a semiconductor substrate;
forming a silicon rich nitride layer over the first dielectric layer;
forming an intermediate layer with a nitride over the silicon rich nitride layer; and

forming a second dielectric layer by *steam oxidizing* the intermediate layer;

wherein the silicon rich nitride layer is situated adjacent to the first dielectric layer and the nitride in the intermediate layer is situated adjacent to the second dielectric layer *so as to cause a charge-storage bi-layer formed by the silicon rich nitride layer and the intermediate layer to have increased data retention.*

Examiner's Rejections

(1) The Examiner rejected claims 1-6 and 10 as being anticipated under 35 U.S.C. § 102(b) by Ramkumar (US 6,828,201 B1). Ans. 3-5.

(2) The Examiner rejected claims 7-9 as being unpatentable under 35 U.S.C. § 103(a) over Ramkumar and Bhattacharya (US 6,339,000 B1). Ans. 5-7.

*Appellants' Contentions*¹

(1) Appellants contend (Br. 7-13), *inter alia*, that the Examiner erred in rejecting claims 1-6 and 10 as being anticipated by Ramkumar because the portions of Ramkumar (col. 4, ll. 23-33; col. 6, ll. 31-33; Figures 4B-4E) cited by the Examiner fail to teach or suggest the specific arrangement and composition of layers set forth in independent claims 1 and 6.

(2) Appellants contend (Br. 14) that the Examiner erred in rejecting claims 7-9 as being unpatentable over the combination of Ramkumar and Bhattacharya for the same reasons provided with respect to the anticipation rejection.

¹ Separate patentability is not argued for claims 2-5, 7-9, and 10, and Appellants rely on the arguments as to claims 1 and 6 (*see* Br. 13 and 14). Accordingly, we decide this appeal on the basis of claims 1 and 6.

Principal Issue on Appeal

Has the Examiner erred in rejecting claims 1-10 as being anticipated or obvious because Ramkumar fails to disclose the specific arrangement for the plurality of layers that make up the “charge-storage bi-layer formed by the charge trap layer and the intermediate layer”, where the charge trap layer is “situated adjacent to” the first insulator/dielectric layer and the intermediate layer is “situated adjacent to” the second insulator/dielectric layer, as recited in independent claims 1 and 6?²

ANALYSIS

The way in which the elements are arranged or combined in the claim must itself be disclosed, either expressly or inherently, in an anticipatory reference. “Anticipation requires the presence in a single prior art disclosure of all elements of a claimed invention *arranged as in the claim.*” *Connell v. Sears, Roebuck & Co.*, 722 F.2d 1542, 1548 (Fed. Cir. 1983) (emphasis added). The requirement that the prior art elements themselves be “arranged as in the claim” means that claims cannot be “treated . . . as mere catalogs of separate parts, in disregard of the part-to-part relationships set forth in the claims and that give the claims their meaning.” *Lindemann Maschinenfabrik GMBH v. Am. Hoist & Derrick Co.*, 730 F.2d 1452, 1459 (Fed. Cir. 1984). “[U]nless a reference discloses within the four corners of the document not only all of the limitations claimed but also all of the limitations *arranged or combined in the same way as recited in the claim*, it cannot be said to prove

² We recognize that Appellants’ arguments (Br. 7-14) present additional issues. We do not reach these additional issues, as the issue concerning whether or not Ramkumar discloses all of the layers as arranged and recited in claims 1 and 6, is dispositive of the appeal.

prior invention of the thing claimed and, thus, cannot anticipate under 35 U.S.C. § 102.” *Net MoneyIN, Inc. v. VeriSign, Inc.*, 545 F.3d 1359, 1371 (Fed. Cir. 2008) (emphasis added).

In view of the requirement that an anticipatory reference disclose all of the claimed limitations arranged in the same way as recited in the claim (discussed *supra*), we find that Ramkumar fails to disclose all of the steps of forming the four layers, including the charge-storage bi-layer formed of a charge trap layer (claim 1) or silicon-rich nitride layer (claim 6) in combination with an intermediate layer, as recited and arranged as in independent claims 1 and 6.

Ramkumar’s disclosure that the nitride layer 406 is composed of a plurality of layers (*see* col. 6, ll. 31-33) does not provide *the specific arrangement of layers* set forth in claims 1 and 6, nor does Ramkumar’s disclosure provide *any* specific arrangement for the plurality of layers that make up nitride layer 406. Ramkumar’s nitride layer 406 is not reasonably equivalent to any of the four layer arrangements recited in claims 1 and/or 6.

This is because Ramkumar’s nitride layer 406 (Fig. 4E) is disclosed as composed of plural layers such as a layer formed of silicon-rich nitride (i.e., charge trap layer or silicon-rich nitride layer) and an intermediate layer formed of silicon nitride (col. 6, ll. 31-33). However, Ramkumar is silent as to how the silicon-rich nitride layer and intermediate layer(s) are arranged in relation to each other. Ramkumar’s Figure 4E is of no avail, and only shows a single nitride layer 406 interposed between tunnel oxide layer 404 and In Situ Steam Generation (ISSG) top oxide layer 408. Ramkumar’s integrated circuit (Fig. 4E) is made by forming a tunnel oxide 404 (i.e., first insulator/dielectric layer 404), a nitride layer 406 which may include

separate silicon nitride or silicon-rich nitride layers (i.e., charge trap layer and intermediate layer(s)), and an ISSG top oxide layer 408 (i.e., second insulator/dielectric layer), in that order (col. 6, ll. 29-36). The layer formations and relationship of the integrated circuit of Ramkumar shown in Figure 4E and described at column 6, lines 27-50 are not arranged or combined in the same way as set forth in independent claims 1 and 6, thus Ramkumar cannot anticipate claims 1-6 and 10. *Lindemann Maschinenfabrik GMBH v. Am. Hoist & Derrick Co.*, 730 F.2d at 1459; *Net MoneyIN, Inc. v. VeriSign, Inc.*, 545 F.3d at 1371.

Ramkumar, taken individually or as combined by the Examiner with Bhattacharya, fails to disclose a memory cell manufacturing method for forming a charge-storage bi-layer interposed between first and second insulator (claim 1) or dielectric (claim 6) layers, where the charge-storage bi-layer is arranged in two layers made of different materials and formed sequentially over the first insulator/dielectric layer, e.g., silicon-rich nitride and stoichiometric silicon nitride, as set forth in claims 1-6 and 10. Appellants' arguments (Br. 10-14) that Ramkumar (as to claims 1 and 6), and thus the combination relying on Ramkumar as to claims 7-9, fails to disclose or suggest *any specific arrangement* of layers when the nitride layer 406 includes more than one layer (as recited in claims 1 and 6) are therefore persuasive.

Because we agree with Appellants' arguments that Ramkumar, applied by the Examiner as an anticipatory reference, fails to disclose forming the layers as arranged and recited in claims 1 and 6, we will not sustain the Examiner's anticipation rejection of independent claims 1 and 6 based on Ramkumar. For similar reasons, we will not sustain the

Examiner's anticipation rejection of claims 2-5 which depend from claim 1, as well as claim 10 which depends from claim 6.

Appellants' arguments as to dependent claims 7-9 (Br. 14) are persuasive for similar reasons as independent claim 6 from which claims 7-9 depend, and because Bhattacharya fails to cure the noted deficiencies with regard to Ramkumar. Because the Examiner's obviousness rejection of claims 7-9 relies upon the erroneous findings made in the anticipation rejection with regard to Ramkumar's disclosure of the memory cell manufacturing method including the steps of forming the layers as arranged and recited in claim 6 (*see* Ans. 7, "Ramkumar discloses the manufacturing method as claimed in claim 6"), we will not sustain the Examiner's obviousness rejection based on Ramkumar in combination with Bhattacharya.

CONCLUSIONS

(1) Ramkumar fails to disclose the method of manufacturing a memory cell including forming the layers as set forth in independent claim 1 because Ramkumar does not disclose the first insulator layer, charge trap layer, intermediate layer, and second insulator layer as arranged in claim 1.

(2) Ramkumar fails to disclose the method of manufacturing a memory cell including forming the layers as set forth in independent claim 6 because Ramkumar does not disclose the first dielectric layer, silicon-rich nitride layer, intermediate layer, and second dielectric layer as arranged in claim 6. Bhattacharya fails to cure the noted deficiencies with regard to Ramkumar for claims 1 and 6. Appellants have established that the

Examiner erred in rejecting claims 1-10 as being unpatentable under 35 U.S.C. §§ 102(b) and 103(a).

(3) The Examiner erred in rejecting claims 1-6 and 10 under 35 U.S.C. § 102(b) as being anticipated by Ramkumar, and as a result also erred in rejecting claims 7-9 under 35 U.S.C. § 103(a) as being unpatentable over Ramkumar and Bhattacharya.

(4) On this record, claims 1-10 have not been shown to be unpatentable.

DECISION³

The Examiner's rejections of claims 1-10 are reversed.

REVERSED

³ The Patent Trial and Appeal Board is a review body, rather than a place of initial examination. We leave to the Examiner to consider the appropriateness of further rejections of independent claims 1-6 and 10 under 35 U.S.C. § 103(a) over Ramkumar alone. We note that Ramkumar discloses that “nitride layer **406** may include silicon nitride (Si_3N_4), silicon oxynitride, and/or silicon-rich nitride, *in one or more layers*” (col. 6, ll. 31-33) (italicized emphasis added). Thus, Ramkumar suggests forming a charge-storage bi-layer by forming a nitride layer 406 and an intermediate layer over the nitride trap layer (i.e., nitride layer 406 may be composed of several layers, therefore Ramkumar suggests forming an intermediate layer under the condition that nitride layer 406 be composed of a plurality of layers) similar to the recited subject matter of independent claims 1 and 6. Furthermore, (i) Ramkumar’s nitride layer 406 can be a silicon-rich nitride layer (Ramkumar, *see* col. 6, l. 33 suggesting the use of “silicon-rich nitride” for forming nitride layer 406) as recited in claim 2; and (ii) the intermediate layer can be a stoichiometric silicon nitride (Ramkumar, *see* col. 6, l. 32 suggesting the use of “silicon nitride (Si_3N_4)” for forming the suggested intermediate layer) as recited in claim 3.

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