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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte TOSHIYUKI NISHIHARA and
YOSHIO SAKAI

Appeal 2011-002090
Application 11/251,867
Technology Center 2100

Before ROBERT E. NAPPI, HUNG H. BUI, and LYNNE E. PETTIGREW,
Administrative Patent Judges.

BUI, *Administrative Patent Judge.*

DECISION ON APPEAL

Appellants¹ seek our review under 35 U.S.C. § 134(a) of the Examiner's final rejections of claims 41 and 44-66.² We have jurisdiction under 35 U.S.C. § 6(b).

We AFFIRM-IN-PART.³

¹ Real Party in Interest is Sony Corporation.

² Claims 1-40 and 42-43 have been cancelled and are not on appeal.

STATEMENT OF THE CASE

Appellants' Invention

According to Appellants, their invention relates to a storage device able to make a redundant write operation of unselected data unnecessary and able to optimize an arrangement of pages to a state having a high efficiency for rewriting. *See* Appellants' Spec. 14:21-25. The storage device has a first memory unit, a second memory unit having a different access speed from the first memory, and a control circuit configured to move data in two ways between the first memory unit and the second memory unit having different access speeds for reading or rewriting. *Id.*, FIG. 6, and Abstract.

Claims on Appeal

Claims 41 and 44 are the only independent claims on appeal. Claims 41 and 44 are representative of the invention, as reproduced below with disputed limitations emphasized:

41. A storage device comprising:

a first memory unit;

a second memory unit having an access speed higher than said first memory unit, an address conversion table being within said second memory unit; and

³ Our decision refers to Appellants' Appeal Brief filed April 20, 2010 ("App. Br."); Reply Brief filed August 20, 2010 ("Reply Br."); Examiner's Answer mailed July 8, 2010 ("Ans."); Final Office Action mailed October 13, 2009 ("FOA."); and the original Specification filed October 18, 2005 ("Spec.").

a control circuit adapted to control movement of data between said first memory unit and said second memory unit, said data being in units of pages,

wherein said control circuit updates said address conversion table, said address conversion table indicating a correspondence between a page address of said data and an actual location of said data within said first or second memory units,

wherein the first memory unit includes a non-volatile memory, and *the second memory unit includes a non-volatile memory using a ferroelectric material, a phase change material, a ferromagnetic material, or a magnetoresistance effect material for the memory element.*

44. A storage device comprising:

an *address conversion table* configured to store physical addresses of data;

a location in main memory configured to store said data, *said location in the main memory being identifiable by one of the physical addresses;*

a location in auxiliary memory configured to store said data, *said location in the auxiliary memory being identifiable by another of the physical addresses,*

wherein said auxiliary memory has an access speed higher than said main memory.

Evidence Considered

The prior art relied upon by the Examiner in rejecting the claims on appeal is:

Wilson	US 2003/0005249 A1	Jan. 2, 2003
Coulson	US 2005/0138296 A1	Jun. 23, 2005
Shimada	US 2007/0250665 A1	Oct. 25, 2007
Lewis	US 2009/0210623 A1	Aug. 20, 2009

Examiner's Rejection

Claims 41 and 44-66 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the combination of Wilson, Shimada, Lewis,⁴ and Coulson.⁵ Ans. 3-11.

ISSUE

Based on Appellants' arguments, the dispositive issue on appeal is whether the Examiner has erred in rejecting claims 41 and 44-46 under 35 U.S.C. § 103(a) as being unpatentable over Wilson, Shimada, Lewis, and Coulson. App. Br. 6-19. In particular, the issue turns on whether the combination of Wilson, Shimada, Lewis and Coulson discloses or suggests several limitations of Appellants' independent claims 41 and 44. *Id.*

⁴ Lewis is cited to support the Examiner's Official Notice taken that it is well known that cache memories are accessed at a higher speed than hard disk drives, or any other memory devices, in response to Appellants' request. Ans. 4, 12; *see* Lewis, ¶[0029].

⁵ Coulson is cited to support the Examiner's Official Notice taken that it is well known that cache memories can take the form of ferroelectric memories. Ans. 5, 14; *see* Coulson, ¶¶[0019]-[0020].

ANALYSIS

We have reviewed the Examiner's rejections in light of Appellants' arguments that the Examiner has erred. Only those arguments actually made by Appellants in the Appeal Brief have been considered. *See* 37 C.F.R. § 41.37(c)(1)(vii).

Initially, we note that Appellants' Amendment After Final filed concurrently with the Reply Brief on August 20, 2010 pursuant to 37 C.F.R. § 41.33(b) in which claims 41, 44-57 and 63-64 are canceled and claims 58, 59, 60, 61, 62, and 65 are rewritten into independent form, has not been considered or entered as a matter of record by the Examiner. As such, Appellants' arguments presented to new claims 58, 59, 60, 61, 62, and 65 in the Reply Brief filed August 20, 2010, and re-presented during the oral hearings scheduled on March 5, 2013 have not been considered and will not be discussed herein.

With respect to independent claim 41, Appellants argue that the Examiner's combination of references fails to disclose: (1) "a second memory unit having an access speed higher than said first memory unit" (App. Br. 8); (2) "an address conversion table being within said second memory unit" (App. Br. 9); and (3) "the second memory unit includes a non-volatile memory using a ferroelectric material, a phase change material, a ferromagnetic material, or a magnetoresistance effect material for the memory element." (App. Br. 10-13).

However, we find none of Appellant's arguments persuasive. First, as correctly found by the Examiner, Wilson discloses a storage system, shown in FIG. 1 reproduced below, comprising a first memory unit (hard disk 130)

and a second memory unit (CPU 102 including cache 140 and translation look-aside buffer “TLB” 150). Ans. 3-4.

FIG. 1 of Wilson is reproduced below.

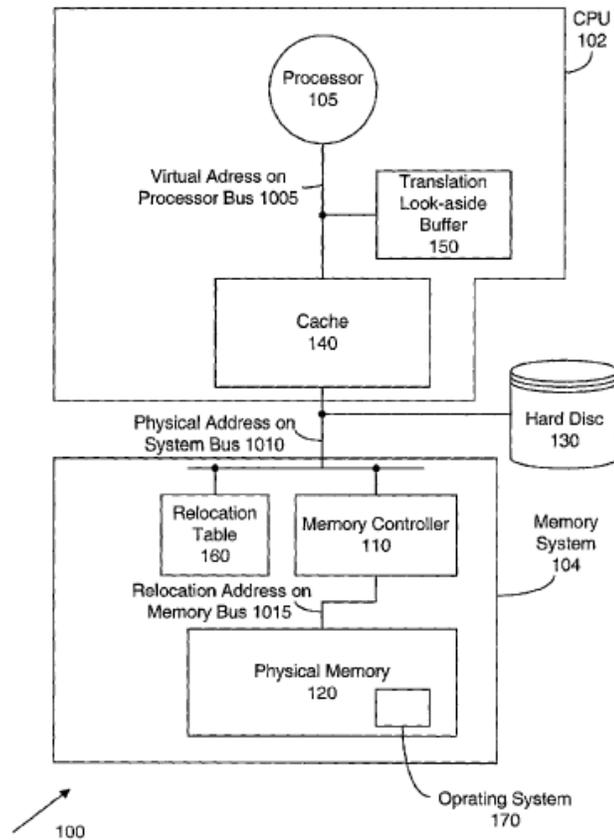


FIG. 1 shows a storage system including 1st memory unit 130 and 2nd memory unit 102.

As shown in FIG. 1, the second memory unit refers to the CPU 102 including cache 140 and TLB 150. The Examiner has taken Official Notice that it is well known that cache memories are accessed at a higher speed than hard disk drives, or any other memory devices. FOA 2; Ans. 4. The Examiner has also cited Lewis to support the Official Notice taken in response to Appellants’ request for evidentiary support. *See* App. Br. 8-9; Ans. 4 (citing Lewis, ¶[0029]); *see also* Shimada, ¶[0003]. Therefore, we

agree with the Examiner that the cache memory 140 of Wilson has a higher access speed than the first memory unit (hard disk 130).

Second, and contrary to Appellants' arguments, both the cache 140 and the TLB 150 of Wilson are stored within the CPU 102, and the CPU 120 is considered as Appellants' claimed "second memory unit." As such, we agree with the Examiner that the TLB 150 of Wilson is within Appellants' claimed "second memory unit."

Third, and as correctly found by the Examiner, the first memory unit of Wilson includes a non-volatile memory. Ans. 5 (citing Wilson, ¶[0056]). Likewise, the second memory unit of Wilson also includes a non-volatile memory. *Id.* The Examiner has taken Official Notice that it is well known that cache memories can take the form of ferroelectric memories, and cited Coulson to support the Official Notice taken. *See* Ans. 5, 13-14 citing Coulson, ¶¶[0019]-[0020]. Therefore, we agree with the Examiner that the cache memory 140 of Wilson can take the form of ferroelectric memories.

For the reasons set forth above, we do not find any error in the Examiner's position and, therefore, sustain the Examiner's obviousness rejection of independent claim 41.

With respect to independent claim 44, Appellants contend that the Examiner's combination of references, including Wilson and Shimada, fails to disclose, among other features: (1) "a location in main memory that is identifiable by a physical address stored within a translation look-aside buffer 150" (App. Br. 14); (2) "a location in auxiliary memory that is identifiable by a physical address stored within a translation look-aside buffer 150" (App. Br. 15); and (3) "physical addresses stored within a translation look-aside buffer 150 identifying locations in ***both*** the hard disk

130 and the cache 140” (App. Br. 15). In particular, Appellants argue that the translation look-aside buffer (TLB) 150 of Wilson is only used to translate data’s virtual address on processor bus 1005 to a physical address on system bus 1010. App. Br. 14

We are persuaded by Appellants’ arguments, and disagree with the Examiner’s factual findings regarding claim 44, and explanations provided in support of the obviousness conclusion (Ans. 7, 14-17). Contrary to the Examiner’s findings, the TLB 150 of Wilson is not capable of storing a physical address to identify locations in both the hard disk 130 and the cache 140, as argued by Appellants. As such, we cannot sustain the Examiner’s obviousness rejection of independent claim 44 as well as its dependent claims 45-66.

CONCLUSION

On the record before us, we conclude that the Examiner has not erred in rejecting claim 41 under 35 U.S.C. § 103(a). However, we also conclude that the Examiner has erred in rejecting claims 44-66 under 35 U.S.C. § 103(a).

DECISION

As such, we AFFIRM the Examiner’s final rejection of claim 41, and REVERSE the Examiner’s final rejection of 44-66.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv) (2011).

AFFIRMED-IN-PART

ELD