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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte JAMES D. PENNOCK, RONALD BAKER,
BRIAN R. PARKER, and CHRISTOPHER BELCHER

Appeal 2011-001738
Application 11/771,764
Technology Center 2100

Before ROBERT E. NAPPI, HUNG H. BUI, and LYNNE E. PETTIGREW,
Administrative Patent Judges.

ROBERT E. NAPPI, Administrative Patent Judge

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134(a) of the rejection of claims 1 through 12, 14, 15, and 17 through 24.

We affirm.

INVENTION

The invention is directed to a communications interface which includes a set of memory spaces which alternately interface with a processor or a serial controller. See paragraphs 0007-0009 of Appellants' Specification. Claim 1 is representative of the invention and reproduced below:

1. An external memory interface engine, comprising:
 - a processor;
 - a memory control subsystem comprising multiple programmable external memory control bits that specify an access operation of multiple different types of external memories;
 - a memory control subsystem comprising:
 - a first memory shared between the processor and the memory control subsystem;
 - a second memory shared between the processor and the memory control subsystem; and
 - a swap controller configured to alternately couple the first memory and the second memory between the processor and the memory control subsystem,where the memory control subsystem is configured to analyze control information and address information stored in the memory subsystem and responsively output the programmable external memory control bits.

REJECTIONS AT ISSUE

The Examiner has rejected claims 1 through 3, 5 through 12, 14, 15, 17, and 18 under 35 U.S.C. § 103(a) as unpatentable over Yoshimura (U.S. Patent 6,421,274 B1) and Keltcher (U.S. Patent 7,043,679 B1). Answer 4-5.¹

The Examiner has rejected claims 4 and 19 through 24 under 35 U.S.C. § 103(a) as unpatentable over Yoshimura, Keltcher, and Hall (U.S. Patent 5,581,779). Answer 8-9.

ISSUE

Appellants argue on pages 9 through 11 of the Appeal Brief that the Examiner's rejection of claims 1 through 3, 5 through 12, 14, 15, 17 and 18 under 35 U.S.C. § 103(a) is in error.² These arguments present us with the issue: did the Examiner err in finding that Yoshimura teaches a controller to alternatively swap access to the first buffer memory and the second buffer memory between the processor and communications subsystem as recited in representative claim 1?

Appellants' argue on pages 11 and 12 of the Brief that the rejection under 35 U.S.C. § 103(a) based upon Yoshimura, Keltcher, and Hall is in error for the same reason as discussed with respect to claim 1. Accordingly, Appellants' arguments directed to the Examiner's rejection under 35 U.S.C. § 103(a) does not present us with any additional issues.

¹ Throughout this opinion we refer to the Examiner's Answer mailed on July 22, 2010.

² Throughout this opinion we refer to Appellants' Appeal Brief filed on May 12, 2010.

ANALYSIS

We have reviewed Appellants' arguments in the Brief, the Examiner's rejection and the Examiner's response to the Appellants' arguments. We disagree with Appellants' conclusion that the Examiner erred in finding that Yoshimura teaches a controller to alternatively swap access to the first buffer memory and the second buffer memory between the processor and communications subsystem. The Examiner has provided a comprehensive response to this issue in the Answer. In particular, the Examiner has found that Yoshimura teaches two memory locations R1 and R2 (see Figure 1) which are alternately connected to a processor or a memory control subsystem. Answer 9-10.

We concur with the Examiner's findings and note that Figures 2A, 2B, 7A, 7B and the accompanying text in Yoshimura provide an example of the alternate access to the memory locations R1 and R2. Based upon these findings, the Examiner concludes that the argued limitation is taught by Yoshimura. We concur with the Examiner's conclusions in the Answer and adopt them as our own. Accordingly, we sustain the Examiner's rejections under 35 U.S.C. § 103(a).

ORDER

The decision of the Examiner to reject claims 1 through 12, 14, 15, and 17 through 24 is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

Appeal 2011-001738
Application 11/771,764

AFFIRMED

ELD