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UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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*Ex parte* JEROEN ANTON JOHAN LEIJTEN<sup>1</sup>

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Appeal 2010-012517  
Application 10/526,421  
Technology Center 2100

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Before JOSEPH F. RUGGIERO, DENISE M. POTHIER, and  
JAMES B. ARPIN, *Administrative Patent Judges*.

ARPIN, *Administrative Patent Judge*.

DECISION ON APPEAL  
STATEMENT OF THE CASE

Appellant appeals under 35 U.S.C. § 134(a) from the Examiner's rejection of claims 1-11, 13, and 15-17. Claims 12 and 14 are cancelled. App. Br. 2.<sup>2</sup> We have jurisdiction under 35 U.S.C. § 6(b). We affirm.

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<sup>1</sup> Koninklijke Philips Electronics N.V. is the real party in interest.

INVENTION

Appellant's invention relates to a data processor comprising one or more functional units, one or more register files, a data memory, and a snapshot buffer that accommodates the storage of state information of the processor during an interrupt condition in respective buffer elements. *See generally* Spec. 1:9-12. Claim 1 is illustrative and is reproduced below with disputed limitations emphasized:

1. A data processor comprising:
  - one or more functional units arranged to provide an internal processor pipeline,
  - one or more register files,
  - a data memory facility having a multibit access port facility,
  - a snapshot buffer, differing from the one or more register files, which during handling of an interrupt condition accommodates saving, by copying from the one or more register files to respective snapshot buffer elements, state information of various processor state elements, *including state information from the internal processor pipeline*, and
  - a controller means arranged to save, upon occurrence of a subsequent interrupt condition during handling of an actual interrupt condition, the state information of various processor state elements currently within the respective snapshot buffer elements in the data memory facility having the multibit access port facility.

The Examiner relies on the following as evidence of unpatentability:

Downing	US 3,781,810	Dec. 25, 1973
Forsyth	US 5,327,566	July 5, 1994
Petolino	US 5,958,041	Sept. 28, 1999

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<sup>2</sup> Throughout this opinion, we refer to (1) the Appeal Brief (App. Br.) filed April 29, 2010; (2) the Examiner's Answer (Ans.) mailed July 16, 2010; and (3) the Reply Brief (Reply Br.) filed September 16, 2010.

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Lang et al., *Individual Flip-Flops with Gates Clock for Lower Power Datapaths*, IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing, Vol. 44, No. 6, (1997), pp. 508-516.

Patterson et al., *Computer Organization & Design: The Hardware/Software Interface*; Morgan Kaufmann Publishers, 2d ed., (1998), pp. 134-135

#### THE REJECTIONS

1. The Examiner rejected claims 1-3, 5-7, 9, 13, and 15-17 under 35 U.S.C. § 103(a) as unpatentable over Downing. Ans. 4-7.
2. The Examiner rejected claim 4 under 35 U.S.C. § 103(a) as unpatentable over Downing, as applied to claim 1, and Petolino. *Id.* at 7-8.
3. The Examiner rejected claim 8 under 35 U.S.C. § 103(a) as unpatentable over Downing, as applied to claim 7, and Patterson. *Id.* at 8-9.
4. The Examiner rejected claim 10 under 35 U.S.C. § 103(a) as unpatentable over Downing, as applied to claim 1, and Forsyth. *Id.* at 9.
5. The Examiner rejected claim 11 under 35 U.S.C. § 103(a) as unpatentable over Downing, as applied to claim 1, and Lang. *Id.* at 9-10.

#### OBVIOUSNESS REJECTION OVER DOWNING

Regarding representative claim 1, the Examiner finds that Downing discloses all of the limitations of the claimed invention, except that Downing does not explicitly disclose that the system is pipelined. Ans. 4.

Nevertheless, the Examiner finds that “the use and benefits of pipelining are

notoriously well known in the art, and the use of the techniques described by Downing in a pipelined processor would . . . have been obvious to a person having skill in the art.” *Id.* at 4-5.

Appellant argues that Downing fails to teach or suggest “saving . . . state information of various processor state elements, *including state information from the internal processor pipeline.*” App. Br. 4, 9 (emphasis added). Instead, Appellant argues that Downing discloses “discarding internal pipeline state information in response to an interrupt,” e.g., flushing. *Id.* at 4 (emphasis omitted).

#### ISSUES

(1) Under § 103, has the Examiner erred in rejecting claim 1 by finding that Downing would have taught or suggested “a snapshot buffer, differing from the one or more register files, which during handling of an interrupt condition accommodates saving, by copying from the one or more register files to respective snapshot buffer elements, state information of various processor state elements, *including state information from the internal processor pipeline*” (emphasis added)?

(2) Is the Examiner’s reason to modify the teachings of Downing supported by articulated reasoning with some rational underpinning to justify the Examiner’s obviousness conclusion?

#### ANALYSIS

We begin by construing the disputed limitation of claim 1 which calls for, in pertinent part, “saving . . . state information of various processor state elements, *including state information from the internal processor pipeline.*” App. Br. 9 (emphasis added). Referring to the claim language, Appellant recites that, during the handling of an interrupt condition, the snapshot buffer

saves state information of various processor state elements. *Id.* The snapshot buffer differs from the one or more register files of the data processor. *Id.* Nevertheless, the snapshot buffer copies the state information of various processor state elements from the one or more register files. *Id.* Further, the state information of various processor state elements includes the state information from the internal processor pipeline. *Id.* Therefore, we construe the claim to include that the snapshot buffer saves state information from the one or more register files while handling an interrupt condition and, thereby, also saves the included state information from the internal processor pipeline.

Appellant indicates that support for this limitation is found at the Specification on page 5, lines 17-22. App. Br. 2; Transcript 5:8-12 (citing Spec. 5:17-19). In particular, with respect to the preferred embodiment of Figure 3, Appellant describes that:

[a]t the start of each interrupt handling, a *complete* snapshot is taken from the relevant processor state within a single clock cycle through instantly copying the value of each normal flipflop to its corresponding shadow flipflop. Similarly, at the end of each interrupt handling, the *complete* snapshot is restored from the snapshot buffer to the processor proper by instantly copying each shadow flipflop to its corresponding normal fiipflop.

Spec. 5:17-22 (emphases added).<sup>3</sup> Although the term “state instructions” does not appear in the cited text; during the oral hearing, Appellant stated that the reference to taking and restoring a “complete” snapshot describes

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<sup>3</sup> Although Appellant refers to “state information” elsewhere in the Specification (Spec. 1:11, 16), Appellant does not expressly define the term. See Transcript 5:5-6:14.

the state information from the internal processor pipeline. Transcript 5:15-22. This is consistent with the claim language reciting that by saving state information by copying from the one or more register files while handling an interrupt condition, the snapshot buffer also saves the included state information from the internal processor pipeline. App. Br. 4-5.

Appellant acknowledges that Downing teaches or suggests that, in a program controlled computer, which comprises independent control circuitry; data is exchanged between registers R1-Rn and the computer memory. App. Br. 5. Further, as the Examiner notes, Downing describes that “[w]hen the first save register contents instruction 2A (FIG. 3) is decoded, . . . the contents of the registers R1 and Rn [are] being stored in the auxiliary registers AR1 and ARn, respectively.” Downing, col. 3, ll. 25-27; *see* Ans. 4. Appellant argues, however, that Downing refers to the exchange of particular data contained in the registers and that such data does not include state information from the internal processor pipeline. App. Br. 5-6; Transcript 9:2-14. Referring to Downing’s Figures 1, 2A, and 2B, Appellant argues that Downing teaches that its processor comprises pipelined elements. App. Br. 6. In particular, Appellant identifies several of Downing’s components that allegedly are internal state elements. *Id.* (identifying SAVR, element 32, RESR, element 33, and Address Register 16); Transcript 10:17-11:6. Thus, Appellant concludes that “Downing handles nested interrupts by saving only register data and *not* internal state information.” Reply Br. 5 (citing App. Br. 6, ll. 4-21). We disagree with this conclusion.

Appellant argues that the *data* transferred between registers R1-Rn to registers AR1-ARn is not *state information*. App. Br. 6, Reply Br. 5.

Nevertheless, Appellant fails to demonstrate that Downing's data excludes all state information or that, to the extent that Downing describes state information, state information is only stored and transferred between the identified, internal state elements, rather than Downing's registers and auxiliary registers. *Id.* During the oral hearing, Appellant acknowledged that Downing does not separately mention state information from the "internal processor pipeline." Transcript 9:22-10:2. Further, referring to the identified, internal state elements, Appellant argues that state information from Downing's internal processor pipeline "must be flushed" because of the interaction of Downing's base address store 30, pointer store 29, and address element 27. App. Br. 6 (citing Downing, Fig. 2B). Nevertheless, this argument is premised on the assumption that Downing's data does not include *any* state information, including *any* state information from the internal processor pipeline. *Id.*; Reply Br. 4. Further, during the oral hearing, Appellant acknowledged that Downing does not separately mention the term "flushing." Transcript 14:11-22 (stating that "Downing isn't even concerned with the issue of the need to flush"). Appellant simply has failed to provide sufficient support for this assumption.

Based on the foregoing analysis, we conclude that Downing's disclosure of transferred data is properly deemed sufficiently broad to teach or suggest state information, including state information from the internal processor pipeline. As the Examiner notes, Downing clearly describes that "the contents of the registers R1 and Rn [are] being stored in the auxiliary registers AR1 and ARn, respectively." Downing, col. 3, ll. 22-27; *see also* Ans. 4 (citing Downing, col. 4, ll. 5-10) (describing transfer of "The contents of the registers R1 and Rn,")). Finally, although not relied upon by the

Examiner, we note that, Downing provides further support for this conclusion, stating that:

[a] “save” instruction provides for the simultaneous transfer of data *from all machine registers* specified by that instruction *to their corresponding auxiliary registers*. Similarly, the “restore” instruction is utilized to simultaneously transfer data *to all machine registers* specified by that instruction *from their corresponding auxiliary registers*.

Downing, col. 1, ll. 54-60 (emphases added). Thus, we find that the Examiner demonstrates that Downing teaches or suggests all of the limitations of claim 1.

During the oral hearing, Appellant also argued that a person of ordinary skill in the relevant art would not have modified Downing to achieve Appellant’s claimed invention because Downing and Appellant’s invention are directed to different problems. Although this argument was not raised in the Appeal or Reply Briefs, Appellant argued that its first presentation during the oral hearing was due to the U.S. Court of Appeals for the Federal Circuit’s recent decision in *Mintz v. Dietz & Watson, Inc.*, 679 F.3d 1372 (Fed. Cir. 2012). Transcript 3:12-4:19. In *Mintz*, the Federal Circuit indicated that the statement of the problem confronted by the applicant can represent a form of prohibited reliance on hindsight. *Id.* at 1377. The Federal Circuit found that:

[t]he district court has used the invention to define the problem that the invention solves. Often the inventive contribution lies in defining the problem in a new revelatory way. In other words, when someone is presented with the identical problem and told to make the patented invention, it often becomes virtually certain that the artisan will succeed in making the invention.

*Id.* Nevertheless, the Examiner does not contend that that Downing and Appellant seek to solve the identical problem. *See KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 420 (2007) (“Under the correct analysis, *any need or problem* known in the field of endeavor at the time of invention and addressed by the patent can provide a reason for combining the elements in the manner claimed.” (emphasis added)). Instead, the Examiner merely states that each of Downing and Appellant applies the same techniques with respect to internal processor pipelining. Ans. 4. Thus, to the extent that Downing is directed to a similar or different problem than Appellant’s invention, the Examiner is not prohibited from basing the rejection of claim 1 on Downing. Therefore, to the extent that Appellant’s argument regarding *Mintz* is not untimely, we find this argument unpersuasive.

For the foregoing reasons, Appellant has not persuaded us of error in the rejection of independent claim 1 and of dependent claims 2, 3, 5-7, 9, 13, and 15-17, which are not separately argued with particularity. App. Br. 7; Reply Br. 4. Therefore, we sustain the obviousness rejection of these claims.

#### THE REMAINING REJECTIONS

Although the Examiner rejects claims 4, 8, 10, and 11 under § 103 as unpatentable over Downing in combination with another reference, each of these claims depends, directly or indirectly, from independent claim 1; and Appellant does not argue any of these claims separately. Reply Br. 4 (claim 1 is “the only claim specifically argued on appeal”). For the foregoing reasons, Appellant has not persuaded us of error in the rejection of independent claim 1. Therefore, we are not persuaded of error in the

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rejections of dependent claims 4, 8, 10, and 11; and we sustain these remaining rejections.

#### CONCLUSION

The Examiner did not err in rejecting claims 1-11, 13, and 15-17 under § 103.

#### DECISION

The Examiner's decision rejecting claims 1-11, 13, and 15-17 is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED

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