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CAREY, RODRIGUEZ, GREENBERG & O'KEEFE, LLP			THOMAS, TOM	
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The time period for reply, if any, is set in the attached communication.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte JIN CAI, WILFRIED E. HAENSCH, TAK H. NING, PHILIP J.
OLDIGES and GHAVAM G. SHAHIDI

Appeal 2010-010252
Application 11/857,569
Technology Center 2800

Before CARL W. WHITEHEAD, JR., ERIC S. FRAHM and ANDREW J.
DILLON, *Administrative Patent Judges*.

WHITEHEAD, JR., *Administrative Patent Judge*.

DECISION ON APPEAL

STATEMENT OF THE CASE

Appellants are appealing claims 1 and 3-19. Appeal Brief 1. We have jurisdiction under 35 U.S.C. § 6(b) (2012).

We affirm.

Introduction

The invention is directed to a series transistor device that reduces Single-Event Upset (SEU). Specification 2-5.

Illustrative Claim

1. A series transistor device, comprising:
a series source;
a series drain;
a first constituent transistor having a first source and a first drain; and
a second constituent transistor having a second source and a second drain, wherein
all of the constituent transistors have a same conductivity type,
the series source is the first source,
the series drain is the second drain, and
a drain of one of the constituent transistors is merged with a source of another of the constituent transistors, wherein
the series transistor device is a SOI device.

Rejections on Appeal

Claims 1, 3, 10, 13-15, 18 and 19 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Iwasa (U.S. Patent Number 5,703,381; issued December 30, 1997) and Morris (U.S. Patent Application Publication Number 2005/0179093 A1; published August 18, 2005). Answer 4-9.

Claims 1, 4-6, 13-15, and 17-19 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Matsuda (U.S. Patent Application Publication Number 2004/0007743 A1; published January 15, 2004) and Iwasa. Answer 9-17.

Claims 7-9 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Morris and Proebsting (U.S. Patent Number 4,714,840; issued December 22, 1987). Answer 17-18.

Claim 11 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Iwasa and Vinal (U.S. Patent Number 5,151,759; issued September 29, 1992). Answer 18-19.

Claim 12 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Vinal and Proebsting. Answer 19-20.

Claim 16 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Morris and Proebsting. Answer 20.

Issue on Appeal

Do Iwasa, Morris, Matsuda, Proebsting and Vinal, either alone or in combination, disclose a series transistor device wherein the device is a SOI device?

ANALYSIS

We have reviewed the Examiner's rejections in light of Appellants' arguments that the Examiner has erred. We disagree with Appellants' conclusions. We concur with the findings and reasons set forth by the Examiner in the action from which this appeal is taken and the reasons set forth by the Examiner in the Answer in response to Appellants' Appeal Brief. However, we highlight and address specific findings and arguments for emphasis as follows.

Appellants contend:

Claim 1 recites a "series transistor device," and to teach the claimed series transistor device, the Examiner relied upon TP1 and TP3 of Iwasa. However, TP 1 and TP3 of Iwasa would not be viewed by one having skilled in the art as a series transistor device. Instead, TP1 and TP3 are two separate transistors in a circuit. A series transistor device has a single gate, source, and drain, which are characteristics of a transistor device. However, TP1 and TP3 have separate gates. Thus, the combination of TP1 and TP3 is not a series transistor device. Similarly, claim 13 recites "an input is directly electrically connected to a gate of the n-channel transistor device and a gate of the p-channel transistor device."

Appeal Brief 7.

The Examiner finds Appellants' definition of series transistor "is not met by claim 1" and Appellants' Specification does not particularly define "a series transistor device." Answer 21. We agree with the Examiner's findings. There is nothing novel about connecting transistors in series. Appellants' arguments are not commensurate with the scope of the claims. Claim 1 only requires transistors that are connected together in a series format. Appellants argue a specific configuration of the transistors connected in series which is not recited in claim 1. *See* Appeal Brief 7.

The Examiner relies upon Matsuda to disclose the claimed input configuration of claim 13; however, Appellants do not address why Matsuda is deficient and fails to disclose the claimed invention. *See* Answer 14; *see also* Appeal Brief 10-19. Therefore we do not find Appellants' arguments in regard to the input configuration to be persuasive.

Appellants further argue that "[t]ransforming a CMOS transistor to a SOI transistor is no insignificant task." Appeal Brief 14. Appellants go on to explain the difficulty of such a task. *Id.* at 14-19. We do not question the difficulty in merging CMOS technology with SOI technology; however, as the Examiner finds, such technology is well known in the art. *See* Answer 22-23.

For the reasons stated above, we affirm the Examiner's rejection of independent claims 1, 11 and 13, as well as those claims dependent therefrom.

DECISIONS

The obviousness rejections of claims 1 and 3-19 are affirmed.

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Application 11/857,569

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv). *See* 37 C.F.R. § 41.50(f).

AFFIRMED

peb