



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/036,461	01/13/2005	Tsuyoshi Kitagawa	7705 US	3660
66638	7590	02/04/2013	EXAMINER	
MICHAEL A. NELSON TEKTRONIX, INC. 14150 SW KARL BRAUN DRIVE P.O. BOX 500, M/S 50-LAW BEAVERTON, OR 97077			BULLOCK JR, LEWIS ALEXANDER	
			ART UNIT	PAPER NUMBER
			2199	
			NOTIFICATION DATE	DELIVERY MODE
			02/04/2013	ELECTRONIC

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

jennifer.parker@tektronix.com  
docketing@techlaw.com

UNITED STATES PATENT AND TRADEMARK OFFICE

---

BEFORE THE PATENT TRIAL AND APPEAL BOARD

---

*Ex parte* TSUYOSHI KITAGAWA

---

Appeal 2010-008883  
Application 11/036,461  
Technology Center 2100

---

Before ROBERT E. NAPPI, JUSTIN BUSCH, and BARBARA A.  
PARVIS, *Administrative Patent Judges*.

PARVIS, *Administrative Patent Judge*.

DECISION ON APPEAL

Appellant appeals under 35 U.S.C. § 134(a) from the Examiner's decision finally rejecting claims 1, 3, 4 and 6. We have jurisdiction over the appeal under 35 U.S.C. § 6(b). Claims 2 and 5 have been cancelled.

We AFFIRM.

## STATEMENT OF THE CASE

Appellant's invention relates to generating a delayed analog signal corresponding to processed digital data that has a desired delay relative to an analog signal. (Spec. 1, ll. 5-8, Abstract).

## CLAIMED SUBJECT MATTER

Claims 1 and 4 are the independent claims on appeal. Claim 1 is representative of the subject matter on appeal, and recites:

1. A method for generating a delayed analog signal corresponding to processed digital data that has a desired delay relative to an analog signal corresponding to a source digital data comprising the steps of:

digitally calculating the processed digital data from the source digital data in response to a delay control signal corresponding to the desired delay; and

converting the processed digital data into the delayed analog signal using a modified clock having a frequency that is k-times that of a reference clock for the source digital data.

## REJECTIONS

Claims 1, 4 and 6 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Marchetto et al. (U.S. 5,473,638, Dec. 5, 1995; "Marchetto") in view of Hase et al. (U.S. 5,878,097, Mar. 2, 1999; "Hase"). (Answer 3-5).<sup>1</sup>

Claim 3 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Marchetto in view of Hase and Anderson et al. (U.S. 6,005,983, Dec. 21, 1999; "Anderson"). (Answer 5-6).

---

<sup>1</sup> Throughout this opinion we refer to the Examiner's Answer mailed on Feb. 19, 2010.

## ISSUE

Appellant argues on pages 10 through 12 of the Appeal Brief that the Examiner's rejection of independent claim 1 under 35 U.S.C. § 103(a) is in error.<sup>2</sup> These arguments present us with the following issue:

Did the Examiner err in finding that Hase teaches a “modified clock having a frequency that is k-times that of a reference clock for the source digital data” as recited in claim 1?

## ANALYSIS

We have reviewed the Examiner's rejection of claims 1, 3, 4 and 6 in light of Appellant's arguments that the Examiner has erred. We disagree with Appellant's conclusion. We adopt as our own the findings and reasons set forth by the Examiner in the action from which this appeal is taken and the reasons set forth by the Examiner in the Examiner's Answer in response to Appellant's Appeal Brief. However we highlight and address specific findings and arguments regarding claim 1 for emphasis as follows.

### *The rejection of claim 1 under 35 U.S.C. 103(a)*

*Did the Examiner err in finding that Hase teaches a “modified clock having a frequency that is k-times that of a reference clock for the source digital data” as recited in claim 1?*

The Examiner correctly pointed to excerpts of Hase showing that Hase teaches the “modified clock having a frequency that is k-times that of a reference clock for the source digital data” as recited in claim 1. (Answer 4,

---

<sup>2</sup> Throughout this opinion we refer to Appellant's Appeal Brief filed Dec. 7, 2009.

6-7). Appellant contends that “Hase’s ‘error signal’ does not have a ‘frequency’ at all....” (Appeal Br. 12). However, Appellant did not provide sufficient explanation or analysis in the Appeal Brief to persuade us of error in the Examiner’s rejection of claim 1.

For example, Appellant contends that the Examiner erred in finding that Hase teaches this limitation because the control signal 12 referred to by the Examiner “is not phase-locked and harmonically related to reference signal 7.” (Appeal Br. 11). As support, Appellant refers to one excerpt of Hase relating to Figure 7, but Appellant does not address the following later excerpt regarding this same embodiment. (Appeal Br. 10-11).

The constituent components collectively form a phase-locked loop for producing a control signal 12 to generate an amount of delay independent of variation in quality of the circuit chip, change in power, and deviation in temperature.

(Hase col. 7, ll. 2-5).

Additionally, the Examiner stated:

[T]he secondary reference by Hase et al. clearly disclose[s] the limitations of “converting the processed digital data into the delayed analog signal using a modified clock having a frequency that is k-times that of a reference clock for the source digital data” wherein the modified clock signal is the signal of the PLLs 3-4 in Figures 2-3, particularly the output clock signal of the PLL 4 in Figures 3-4.

(Answer 7). Appellant did not provide sufficient explanation or analysis to persuade us that the Examiner failed to show that PLL 4 in Figures 3-4 meets this limitation. Accordingly, because we are not persuaded of error in the Examiner’s rejection of claim 1 under 35 U.S.C. § 103(a), we sustain the rejection.

Appeal 2010-008883  
Application 11/036,461

*The rejection of claims 3, 4 and 6 under 35 U.S.C. 103(a)*

Appellant did not provide sufficient explanation or analysis in the Appeal Brief regarding the additional arguments relating to claim 3 to persuade us of error in the Examiner's rejection of claim 3. (Appeal Br. 12). With respect to the rejection of claims 4 and 6, Appellant allows those claims to fall with claim 1 by relying on the same reasons presented for the patentability of claim 1. (Appeal Br. 10-12). Accordingly, we sustain the Examiner's rejection of claims 3, 4 and 6 under 35 U.S.C. § 103(a).

CONCLUSION

Based on the record before us, we conclude that the Examiner did not err in rejecting claim 1 as being unpatentable under 35 U.S.C. § 103(a) over Hase and Marchetto. Therefore, we sustain the 35 U.S.C. § 103(a) rejection of claim 1 and of claims 3, 4 and 6 falling therewith.

DECISION

We affirm the Examiner's rejection of claims 1, 3, 4 and 6.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a). *See* 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED

tj