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UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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*Ex parte* ATUL GARG and SIAW-KANG LAI

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Appeal 2010-008693  
Application 10/818,017  
Technology Center 2400

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Before: DAVID M. KOHUT, JASON V. MORGAN, and  
MICHAEL J. STRAUSS, *Administrative Patent Judges*.

STRAUSS, *Administrative Patent Judge*.

DECISION ON APPEAL

STATEMENT OF CASE

Appellants appeal under 35 U.S.C. § 134 from a rejection of claims 1, 3-4, 6-7, and 9-12.<sup>1</sup> Claims 2, 5, and 8 have been canceled. We have jurisdiction under 35 U.S.C. § 6(b).

We AFFIRM-IN-PART and ENTER A NEW GROUND OF REJECTION PURSUANT TO 37 C.F.R §41.50(b).

The claims are directed to a method of improving operational speed of an encryption engine. Claim 1, reproduced below, is illustrative of the claimed subject matter:

1. A method of implementing a function the running of which is based on an input of a first variable which may have a first or a second value, and an input of a second variable which may have a first or a second value, comprising:
  - setting the value of the second variable to the first or the second value thereof;
  - running the function based on an input of the first variable set at the first value thereof,
  - and an input of the second variable having said set value thereof, to provide a first output;
  - running the function based on an input of the first variable set at the second value thereof,
  - and an input of the second variable having said set value thereof, to provide a second output.

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<sup>1</sup> Appellants include in their Reply Brief a request (Reply Br. 2) that prosecution be re-opened in view of the Examiner's withdrawal of the finality of the April 28, 2009 Office Action. However, since Appellants did not file a response under 37 C.F.R. § 1.111 to the Non-Final Office Action of Jul. 30, 2009 and instead filed the subject Appeal Brief on Nov. 13, 2009 and Reply Brief on Mar. 19, 2010, we have decided the appeal on the merits.

## REFERENCES

The prior art relied upon by the Examiner in rejecting the claims on appeal is:

Andreev                      US 6,536,016 B1              Mar. 18, 2003

## REJECTION

The Examiner rejected claims 1, 3-4, 6-7, and 9-12 under 35 U.S.C. § 102(b) as being anticipated by Andreev. Ans. 3.

## APPELLANTS' CONTENTIONS<sup>2</sup>

1. With respect to claims 1, 4 and 7, “the truth table disclosure [according to Table 1A of Andreev] does not disclose [the] requirement of ‘setting’ one of the AND gate input variables to a ‘set value’ and then separately running the AND gate function twice, once with the other input variable set to a first value, and again with the other input variable set to a second value.” App. Br. 7-8; Reply Br. 2-3.

2. With respect to claims 3, 6, 9 and 10, in contrast to Andreev, “the claimed input variables are not complementary to one another since, according to the claims, they each may have ‘a first or second value’” and while “Andreev is concerned with determining if the logic cell is a ‘constant function’ (e.g., a cell whose function does not change), . . . claim 3 provides a way for using the value of the first input variable to choose between two

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<sup>2</sup> Appellants additionally contend that the finality of the April 28, 2009 Office Action was premature. App. Br. 5. This issue was rendered moot by the Examiner’s withdrawal of the finality of the Office Action with issuance of the Non-Final Rejection of Jul. 30, 2009. Furthermore, we note that the finality of an Office Action is not appealable, review of the decision instead available by petition. *See* MPEP §§ 706.07(c) and 1002.02(c)3(a).

possible outputs of the function, which would seem to be the exact reverse of a ‘constant function.’” App. Br. 8, 10.

3. Further with respect to claims 4 and 7, each “includes a third variable in the process which is not disclosed in Andreev.” App. Br. 9.

4. With respect to claim 10, “there does not appear to be any teaching or suggestion of selecting between the third or the fourth output from the second logic block function based on the actual value of the first input variable to the second logic block.” App. Br. 10.

5. With respect to claim 11, Andreev “in no way discloses or suggests that the functions of the first and second logic blocks are run in parallel.” App. Br. 10.

6. With respect to claim 12 Andreev provides “no disclosure or suggestion of using the same function for the first and second logic blocks (as recited in claim 12) when performing the method of implementing functioning of an encryption engine as recited in claim 7.” App. Br. 10.

#### ISSUE ON APPEAL

Based on Appellants’ arguments in the Appeal Brief (App. Br. 7-11) and Reply Brief (Reply Br. 2-4) the issue presented on appeal is whether Andreev discloses the invention as recited in the disputed claims.

#### ANALYSIS

We have reviewed the Examiner’s rejections in light of Appellants’ arguments that the Examiner has erred.

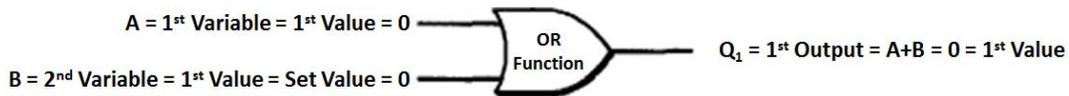
We agree with Appellants’ conclusions as to the rejections of claims 10-12. We disagree with Appellants’ conclusions as to the rejections of

claims 1, 3, 4, 6, 7, and 9 and, in connection with those claims, adopt as our own (1) the findings and reasons set forth by the Examiner in the action from which this appeal is taken and (2) the reasons set forth by the Examiner in the Examiner's Answer in response to Appellants' Appeal Brief and furthermore concur with the conclusions reached by the Examiner. We highlight the following arguments for emphasis.

In connection with contention 1, Appellants argue "the truth table disclosure [according to Table 1A of Andreev] does not disclose [the] requirement of 'setting' one of the AND gate input variables to a 'set value' and then separately running the AND gate function twice, once with the other input variable set to a first value, and again with the other input variable set to a second value." App. Br. 7-8; Reply Br. 2-3. The Examiner responds by referring Appellants to "other different tables" including Table 1B-3A (Ans. 7) "which emphasis different scenarios and appellant does not consider those." More particularly the Examiner considers the logical "OR" functions of Table 1C with inputs A and B mapping to the claimed first and second variables, an input value of "0" to the "first value," "1" to the "second value" and Q to the output. Ans. 8. The mapping is shown graphically with respect to Fig. 1C and Table 1C of Andreev is depicted in the following schematic diagrams as follows.

In particular, "running the function based on an input of the first variable set at the first value thereof, and an input of the second variable having said set value thereof, to provide a first output" is represented by an OR gate having a first input "A" corresponding to the claimed first variable set to a first value of zero, a second input "B" corresponding to the claimed second variable set to a first value (or "set value") of zero, and an output

“ $Q_1$ ” corresponding to the claimed first output equal to the logical OR of the first and second inputs (represented as “ $A+B$ ”) which, in the present case is equal to zero ( $0 + 0 = 0$ ) which is also equal to the claimed first value of zero :



The claim language, “running the function based on an input of the first variable set at the second value thereof, and an input of the second variable having said set value thereof, to provide a second output” is represented by an OR gate having a first input “A” corresponding to the claimed first variable set to a second value of one, a second input “B” corresponding to the claimed second variable set to the “set value” of zero, and an output “ $Q_2$ ” corresponding to the claimed second output equal to the logical OR of the first and second inputs (again represented as “ $A+B$ ”) which, in the present case is equal to one ( $1 + 0 = 1$ ) which is also equal to the claimed second value of one:



See Ans. 8-10.

Appellants reply that “[e]ven assuming that Andreev’s disclosed OR gate function is based on first and second input variables, the truth table disclosure does not disclose claim 1’s requirement of ‘setting’ one of the OR gate input variables to a ‘set value’ and then separately running the OR gate function twice, once with the other input variable set to a first value, and

again with the other input variable set to a second value.” Reply Br. 2.<sup>3</sup> We find Appellants’ argument lacking sufficient evidence to persuade us of Examiner error.

During examination of a patent application, pending claims are given their broadest reasonable construction consistent with the specification. *In re Prater*, 415 F.2d 1393, 1404-05 (CCPA 1969); *In re Am. Acad. of Sci. Tech Ctr.*, 367 F.3d 1359, 1369 (Fed. Cir. 2004). Furthermore, limitations appearing in the specification but not recited in the claim are not read into the claim. *E-Pass Techs., Inc. v. 3Com Corp.*, 343 F.3d 1364, 1369 (Fed. Cir. 2003) (claims must be interpreted “in view of the specification” without importing limitations from the specification into the claims unnecessarily). Thus, while Appellants argue that Andreev does not disclose “setting” OR gate inputs, Appellants’ Specification does not provide a definition of what is meant by “setting.” We instead find it reasonable that Andreev’s truth tables indicating that an input variable has some specified condition<sup>4</sup> such as a value of 0 or 1 meets the requirement for setting the value of a variable, in this case, an input to the disclosed logic gates. Furthermore, contrary to Appellants’ argument, the disputed claims do not require “separately running the OR gate function twice,” only that the “function” (in the applied example, a logical “OR”) be “run”<sup>5</sup> (another undefined claim term) based on

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<sup>3</sup> To the extent that Appellants believe that that the Examiner introduced a new ground of rejection, such is a petitionable matter, and is therefore not a matter before the Board. *See* MPEP § 1207.03 (IV). Furthermore, any such issue is waived because Appellants did not timely file a petition under 37 C.F.R. § 1.181(a).

<sup>4</sup> Set – to put into some condition, *Webster's encyclopedic unabridged dictionary of the English language*. (1996). New York: Gramercy Books.

<sup>5</sup> Run – to operate or function, *id.*

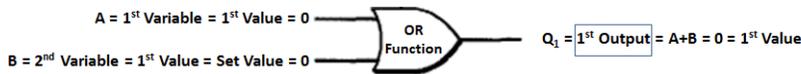
the inputs. Thus, Appellants' arguments are not commensurate in scope with the claims and therefore not persuasive of Examiner error.

Accordingly, giving the claim terminology its broadest reasonable construction consistent with the Specification, we agree with the Examiner that Andreev discloses setting the value of the first and second variables and running a function based on inputs of those variables as required by claims 1, 4 and 7. Since Appellants fail to provide sufficient evidence or argument explaining why Andreev fails to disclose the disputed claim limitations, contention 1 is not persuasive of Examiner error.

In connection with contention 2, Appellants argue that in contrast to Andreev, "the claimed input variables are not complementary to one another since, according to the claims, they each may have 'a first or second value'" and while "Andreev is concerned with determining if the logic cell is a 'constant function' (e.g., a cell whose function does not change), . . . claim 3 provides a way for using the value of the first input variable to choose between two possible outputs of the function, which would seem to be the exact reverse of a 'constant function.'" App. Br. 8. The Examiner responds that the limitations of claim 3 are mapped to Andreev's Table 1C as graphically shown in the following diagrams mapping the language of claim 3 to OR gate circuitry (including the limitations of claim 1.)

In particular, as detailed *supra*, "running the function based on an input of the first variable set at the first value thereof, and an input of the second variable having said set value thereof, to provide a first output" is represented by an OR gate having a first input "A" corresponding to the claimed first variable set to a first value of zero, a second input "B" corresponding to the claimed second variable set to a first value or "set

value” of zero, and an output “ $Q_1$ ” corresponding to the claimed first output equal to the logical OR of the first and second inputs (represented as “ $A+B$ ”) which, in the present case is equal to zero ( $0 + 0 = 0$ ) which is also equal to the claimed first value of zero:



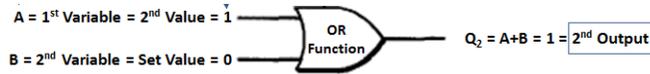
The claim language, “running the function based on an input of the first variable set at the second value thereof, and an input of the second variable having said set value thereof, to provide a second output” is represented by an OR gate having a first input “A” corresponding to the claimed first variable set to a second value of one, a second input “B” corresponding to the claimed second variable set to the “set value” of zero, and an output “ $Q_2$ ” corresponding to the claimed second output equal to the logical OR of the first and second inputs (represented as “ $A+B$ ”) which, in the present case is equal to one ( $1 + 0 = 1$ ) which is also equal to the claimed second value of one may be depicted as:



Claim 3 further requires that the first output [according to the present mapping, having value of zero] being selected if the first variable [“A” in the diagrams] has the first value [0] thereof, which may be shown schematically with inputs to the OR gate both having values of zero with  $Q_1 = 0$  which is also equal to the first output, as follows:



Claim 3 still further requires, in the alternative, the second output [1] being selected if the first variable [A] has the second value [1] thereof , which may be shown schematically with inputs to the OR gate input values having respective values of one and zero with  $Q_2$  equal to one which is also equal to the second output value of one, as follows:



See Ans. 8-11.

We agree with the Examiner that Andreev discloses the limitations of claim 3. While Appellants argue that the Examiner's citation to Andreev at col. 2, ll. 6-19 includes the use of complementary input signals, Table 1C includes no such limitation, instead including all possible logic combinations for the inputs. Thus, while a particular embodiment disclosed by the cited portion of Andreev describes complementary first and variables, the disclosure of Table 1C referenced in the Examiner's Answer does not so limit the inputs. Appellants' further argument attempting to distinguish claim 3 over Andreev based on different concerns to which the respective inventions are directed is equally unpersuasive of error since there is insufficient evidence or argument that these alleged differences are reflected in and/or are supported by specific claim language. Therefore, contention 2 is not persuasive of Examiner error.

In connection with contention 3 Appellants argue that each of claims 4 and 7 "includes a third variable in the process which is not disclosed in Andreev." App. Br. 9. The Examiner cites to Andreev col 4, ll. 55-65 and col. 5, ll. 26-59 for disclosing, *inter alia*, the disputed third variable. Ans. 4. Therein Andreev discloses combinational circuit 40 with primary inputs  $X_1, X_2, \dots, X_{n-1}$ , and  $X_n$  and outputs  $F_1, F_2, \dots, f_{k-1}$ , and  $f_k$ . Andreev col. 4, ll.

60-62. Furthermore Andreev discloses that an example of logical cell c of combinational circuit 40 (referenced as circuit S) has three inputs as depicted in Fig. 5. Thus, we disagree that Andreev fails to disclose the disputed limitation of claims 4 and 7. We add that Andreev's disclosure of multiple inputs to a logic function implies multiple variables. *In re Preda*, 401 F.2d 825, 826 (CCPA 1968)(In determining whether a prior art reference teaches the claimed subject matter under 35 U.S.C. § 102, "it is proper to take into account not only specific teachings of the reference but also the inferences which one skilled in the art would reasonably be expected to draw therefrom."). Since Appellants have failed to provide sufficient evidence or argument in support of contention 3, we find no Examiner error.

In connection with contentions 4-6 Appellants argue that the claim limitations are not disclosed by Andreev. App. Br. 10. The statements of the rejections cite to Andreev col. 8, ll. 7-60 (claim 10), col 9, ll. 7-44 (claim 11) and col. 6, ll. 17-54 without any explanation nor does the Examiner provide any explanation addressing Appellants' contentions in the Response to Argument section of the Answer. We have reviewed the cited portions of Andreev and find nothing therein even suggestive of the claimed limitations. Accordingly, the Examiner's rejection and explanation thereof, on its face, fails to present a convincing case of anticipation of claims 10-12 within the meaning of 35 U.S.C. § 102.

For the reasons discussed *supra*, we sustain the rejections of claims 1, 3-4, 6-7, and 9 under 35 U.S.C. § 102(b) as being anticipated by Andreev and reverse the rejections of claims 10-12.

### NEW GROUND OF REJECTION

The following new grounds of rejection are entered pursuant to 37 C.F.R. § 41.50(b). Claims 1, 3, 4, 6, 7, and 9-12 are rejected under 35 U.S.C. § 101 as being directed towards non-statutory subject matter.

Claims 1, 3, 4, 6, 7, and 9-12 recite a method of implementing a function based on two or more variables which may have respective first and second values. These claims generally recite steps to running the function on different combinations of the values to provide first and second outputs. Dependent claims include selecting an output dependent on an input value and performing the functions simultaneously.

MPEP § 2106 II B<sup>6</sup> “presents factors that are to be considered when evaluating patent-eligibility of method claims.” These factors include:

(a) Whether the method involves or is executed by a particular machine or apparatus.

(b) Whether performance of the claimed method results in or otherwise involves a transformation of a particular article.

(c) Whether performance of the claimed method involves an application of a law of nature, even in the absence of a particular machine, apparatus, or transformation.

(d) Whether a general concept (which could also be recognized in such terms as a principle, theory, plan or scheme) is involved in executing the steps of the method.

MPEP § 2106 II B.

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<sup>6</sup> MPEP §2106 II.B.2; 8th Ed., Rev. 9.

The presence or absence of a single factor will not be determinative as the relevant factors need to be considered and weighed to make a proper determination as to whether the claim as a whole is drawn to an abstract idea. *Id.*

Here, with respect to factor (a) the method does not involve a particular machine or apparatus. Specifically, there are no structural elements recited in claims 1, 3, 4 or 6. Claim 7 and claims 9-12 dependent therefrom generally recite first and second “logic blocks” but fail to set forth a particular machine. With respect to factor (b), while the method steps run logic functions to provide an output, the steps do not involve the transformation of a particular article. Factor (d) further requires inquiry as to whether the concept is abstract and whether the concept is disembodied or implemented in a tangible way. We find that the claimed method is abstract and is not implemented in a tangible manner because there are no structural elements recited to carry out the method steps. As to factor (c), we find that the claims are not drawn to a law of nature. We therefore conclude that claims 1, 3, 4, 6, 7 and 9-12 are not directed towards statutory subject matter.

### CONCLUSION

The Examiner erred in rejecting claims 10-12 under 35 U.S.C. § 102(b) as being anticipated by Andreev.

The Examiner did not err in rejecting claims 1, 3, 4, 6, 7, and 9 under 35 U.S.C. § 102(b) as being anticipated by Andreev.

A new ground of rejection is entered pursuant to 37 C.F.R. § 41.50(b) and claims 1, 3, 4, 6, 7, and 9-12 are rejected under 35 U.S.C. § 101 as being directed towards non-statutory subject matter.

#### DECISION

The decision of the Examiner to reject claims 10-12 is reversed and to reject claims 1, 3, 4, 6, 7, and 9 is affirmed. We enter a new ground of rejection of claims 1, 3, 4, 6, 7 and 9-12.

This decision contains new grounds of rejection pursuant to 37 C.F.R. § 41.50(b). 37 C.F.R. § 41.50(b) provides “[a] new ground of rejection pursuant to this paragraph shall not be considered final for judicial review.”

37 C.F.R. § 41.50 (b) also provides that the appellant, WITHIN TWO MONTHS FROM THE DATE OF THE DECISION, must exercise one of the following two options with respect to the new ground of rejection to avoid termination of the appeal as to the rejected claims:

(1) *Reopen prosecution.* Submit an appropriate amendment of the claims so rejected or new evidence relating to the claims so rejected, or both, and have the matter reconsidered by the examiner, in which event the proceeding will be remanded to the examiner ....

(2) *Request rehearing.* Request that the proceeding be reheard under § 41.52 by the Board upon the same record ....

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

Appeal 2010-008693  
Application 10/818,017

AFFIRMED-IN-PART;

37 CFR § 41.50(b)

msc