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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte OLIVER P. SOHM

Appeal 2010-008555
Application 11/383,465
Technology Center 2100

Before HOWARD B. BLANKENSHIP, MICHAEL R. ZECHER, and
GLENN J. PERRY, *Administrative Patent Judges*.

ZECHER, *Administrative Patent Judge*.

DECISION ON APPEAL

I. STATEMENT OF THE CASE

Appellant appeals under 35 U.S.C. § 134(a) from the Examiner's rejection of claims 1-12. App. Br. 5.¹ We have jurisdiction under 35 U.S.C. § 6(b).

We affirm.

Appellant's Invention

Appellant invented a system, method, and computer-readable medium for executing a series of instructions on a circuit. Spec. ¶ [0006]. According to Appellant, the claimed invention includes an encoder that receives data corresponding to the executed instructions, groups the event data into one or more groups, and outputs the highest priority for each group. *Id.*

Illustrative Claim

Claims 1, 8, and 12 are independent claims. Independent claim 1 is illustrative:

1. A system comprising:
a circuit configured to execute a series of instructions;
and
an encoder configured to receive event data corresponding to the executed series of instructions, said event data describes at least processor stalls;
wherein, said encoder groups the received event data into one or more groups and outputs a highest priority event for each group as prioritized event data; and
wherein said encoder provides said highest priority event to a computer external to said system.

Prior Art Relied Upon

Dreyer	US 5,657,253	Aug. 12, 1997
Izzard	US 6,170,032 B1	Jan. 2, 2001

¹ All references to the Appeal Brief refer to the Appeal Brief filed February 3, 2010, which replaced the Appeal Brief filed January 18, 2010.

Swoboda	US 2001/0039488 A1	Nov. 8, 2001
Swaine	US 2003/0229823 A1	Dec. 11, 2003
Sohm	US 7,334,114 B2	Feb. 19, 2008

(effectively filed May 16, 2005)

“*Coresight*[™] v.1.0 Architecture Specification” (ARM Limited)(2004)
(hereinafter “ARM”).

Rejection on Appeal

Claims 1-12 were rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 5 of U.S. Pat. No. 7,334,114. Ans. 3-10.

Claims 1-12 were rejected under 35 U.S.C. § 103(a) as being unpatentable over the combination of Swoboda, Dreyer, Izzard, and Swaine. *Id.* at 10-14.

Claims 1-12 were rejected under 35 U.S.C. § 103(a) as being unpatentable over the combination of ARM and Dreyer. *Id.* at 14-17.

Examiner’s Findings and Conclusions

1. The Examiner finds that the invention of Swoboda is directed toward a flexible, programmable debug system. Ans. 24. The Examiner finds that replacing Swoboda’s OR gate with Izzard’s priority encoder only changes the manner in which the event data is ultimately output, e.g., output data would indicate the highest priority event occurring rather than indicate that an event occurred, and does not teach away from Swoboda’s intent of a flexible, programmable debug system. *Id.* Moreover, the Examiner finds that Swoboda refers to the OR gate as an example and not as a requirement to fulfill an inventive concept of generating a combined trigger output signal. *Id.* (citing to ¶ [0111].) Further, the Examiner finds that Swaine

teaches avoiding overflow of a trace device by outputting only high priority signals amongst many trace signals. *Id.* at 25 (citing to ¶¶ [0007], [0011], and [0013]). Based upon Swaine’s teachings, the Examiner concludes that one with ordinary skill in the art at the time of the invention would have been motivated to use Izzard’s priority encoder circuit in the invention of Swoboda in order to avoid overflow. *Id.*

2. The Examiner takes the position that ARM’s trace funnel constitutes the claimed “encoder.” Ans. 26-27. Next, the Examiner cites to ARM’s trace sink with the intent of showing how the trace funnel provides the highest priority event to a computer external to the system, as required by independent claims 1, 8, and 12. *Id.* at 28. After citing to various disclosures within ARM, the Examiner ultimately finds that ARM’s debugger is the computer external to the system and is connected to the trace funnels via the trace sink. *Id.* at 28-29 (citing to pg. 17-7, section 13.1, Glossary-6, and pg. 1-9).

Appellant’s Contentions

1. Appellant disagrees with the Examiner’s position that it would have been obvious to replace OR gate 121 illustrated in Swoboda’s Figure 12 with Izzard’s priority encoder in order to teach “said encoder . . . outputs a highest priority event for each group as prioritized event data[,]” as recited in independent claim 1. App. Br. 12; Reply Br. 2. Appellant contends that replacing Swoboda’s OR gate 121 with Izzard’s priority encoder would prevent Swoboda from being able to generate the combined trigger output signal 123 because Izzard’s priority encoder has no ability to logically combine the various inputs into a single output signal. App. Br. 12. Moreover, Appellant argues that because priority does not appear to be

relevant to the operation of Swoboda's system, the only reason to introduce Izzard's priority encoder into Swoboda's system would be based on impermissible hindsight reconstruction. Reply Br. 2. Further, Appellant contends that the Examiner's rationale for combining Swoboda, Dreyer, and Izzard is flawed because Swaine does not disclose any motivation for using a priority encoder to avoid overflow at a trace receiving device, let alone a need to prioritize signals. App. Br. 12-13. Moreover, Appellant asserts that Swaine already indicates a solution to the problem of the overflow of trace signals. *Id.* at 13 (citing to ¶¶ [0009], [0011-13]).

Appellant relies upon the same arguments presented for the obviousness rejection of independent claim 1 to rebut the obviousness rejections of independent claims 8 and 12. *Id.*

2. Appellant contends that ARM's trace funnel only provides an output to an internal embedded trace buffer or a trace port interface unit, and does not provide a highest priority event to an external computer. Reply Br. 2. Therefore, Appellant asserts that ARM does not teach "said encoder provides said highest priority event to a computer external to said system[,]" as recited in independent claim 1, and similarly recited in independent claims 8 and 12. *Id.*

II. ISSUES

1. Has the Examiner erred in determining that the combination of Swoboda, Dreyer, Izzard, and Swaine renders independent claims 1, 8, and 12 unpatentable? In particular, the issue turns on whether:

(a) the combination of Swoboda, Dreyer, and Izzard collectively teaches "[the] encoder . . . outputs a highest priority event for each group as

prioritized event data[.]” as recited in independent claim 1, and similarly recited in independent claims 8 and 12; and

(b) the Examiner provides an articulated reason with a rationale underpinning to support the legal conclusion of obviousness.

2. The dispositive issue before us is whether the Examiner erred in determining that the combination of ARM and Dreyer collectively teaches that “[the] encoder provides [the] highest priority event to a computer external to [the] system[.]” as recited in independent claim 1, and similarly recited in independent claims 8 and 12?

III. ANALYSIS

Obviousness-Type Double Patenting Rejection

Because Appellant does not present any arguments with respect to the Examiner’s obviousness-type double patenting rejection of claims 1-12 as being unpatentable over claim 5 of U.S. Pat. No. 7,334,114, we summarily sustain the obviousness-type double patenting rejection of those claims.²

35 U.S.C. § 103(a) Rejection—Combination of Swoboda, Dreyer, Izzard, and Swaine

Claims 1, 8, and 12

Based on the record before us, we do not discern error in the Examiner’s obviousness rejection of independent claim 1, which recites, *inter alia*, “[the] encoder . . . outputs a highest priority event for each group as prioritized event data[.]” We also do not discern error in the Examiner’s

² See Manual of Patent Examining Procedure § 1205.02, 8th ed., Rev. 8, July 2010 (“If a ground of rejection stated by the examiner is not addressed in the appellant’s brief, that ground of rejection will be summarily sustained by the Board.”).

obviousness rejection of independent claims 8 and 12, which recite a similar claim limitation.

We begin our analysis by reviewing the textual portions of both Swoboda and Izzard relied upon by the Examiner to collectively teach the disputed claim limitation. The Examiner relies upon Figure 12 of Swoboda, which illustrates inputting signals from a plurality of trigger builders into an OR gate to produce a combined trigger signal. Ans. 10 (citing to ¶ [0111]). The Examiner then proceeds to rely upon Izzard's priority encoder circuit, which outputs the highest priority input for each group of prioritized data. *Id.* at 12 (citing to Fig. 1). Based on those cited disclosures, the Examiner takes the position that Izzard's priority encoder circuit is capable of being substituted for Swoboda's OR gate in order to output the highest priority event. *See id.* at 24. We agree with the Examiner.

Other than generally allege that the operation of Swoboda's system is not relevant to priority (Reply Br. 2), Appellant does not provide a reasoned explanation indicating why such a substitution would have been uniquely challenging or otherwise beyond the level of an ordinarily skilled artisan. *See Leapfrog Enters., Inc. v. Fisher-Price, Inc.*, 485 F.3d 1157, 1162 (Fed. Cir. 2007). Moreover, as discussed *supra*, the Examiner's position is properly supported by underlying factual findings. Therefore, contrary to Appellant's argument (Reply Br. 2), we have no reason to believe that the Examiner engaged in impermissible hindsight reconstruction. As a result, the Examiner's reliance on the collective teachings of Swoboda and Izzard properly accounts for the disputed claim limitation.

Rationale to Combine

We are not persuaded by Appellant’s argument that the Examiner’s rationale for combining Swoboda, Dreyer, and Izzard using motivation from Swaine is flawed. App. Br. 12-13. Upon reviewing the record before us, we conclude that the Examiner’s suggestion, as disclosed in Swaine, for modifying Swoboda with both Izzard and Dreyer suffices as an articulated reason with a rational underpinning to justify the legal conclusion of obviousness. That is, one with ordinary skill in the art of debugging circuits, at the time of the claimed invention, would have combined Swoboda’s emulation system (¶ [0065]), with Dreyer’s event data that describes processor stalls (Appendix 1—col. 6) and Izzard’s priority encoder circuit (Fig. 1; col. 3, 1. 1-col. 4, 1. 2). That proffered combination would predictably result in avoiding overflow of a trace receiving device by outputting only a high priority signal amongst a plurality of trace signals. *See Swaine* ¶¶ [0007], [0011], [0013].

In addition, the mere substitution of Izzard’s priority encoder circuit (Fig. 1) for Swoboda’s OR gate (¶ [0111]) predictably uses prior art elements according to their established functions—an obvious improvement. *See KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 417 (2007). It follows that the Examiner has not erred in concluding that the combination of Swoboda, Dreyer, Izzard, and Swaine renders independent claims 1, 8, and 12 unpatentable.

Claims 2-7 and 9-11

Appellant does not provide separate and distinct arguments for patentability with respect to dependent claims 2-7 and 9-11. *See App. Br. 10-13; Reply Br. 1-2.* Therefore, we accept Appellant’s grouping of these

dependent claims with their underlying base claim. App. Br. 13. Consequently, dependent claims 2-7 and 9-11 fall with independent claims 1 and 8, respectively. See 37 C.F.R. § 41.37(c)(1)(vii).

35 U.S.C. § 103(a) Rejection—Combination of ARM and Dreyer

Claims 1, 8, and 12

Based on the record before us, we discern error in the Examiner's obviousness rejection of independent claim 1, which recites, *inter alia*, "[the] encoder provides [the] highest priority event to a computer external to [the] system." We also discern error in the Examiner's obviousness rejection of independent claims 8 and 12, which recite a similar claim limitation.

At the outset, we note that the Examiner relies upon various disclosures within ARM, including ARM's advanced single core trace that provides full trace capabilities in a single processor system (pg. 17-7), before ultimately finding that ARM's debugger is the computer external to the system and is connected to the trace funnels via the trace sink. Ans. 28-29. However, because ARM's single core trace appears to be limited to a single processor system, it is not apparent to us how the output of that trace eventually ends up at an external computer—in this case ARM's debugger.

Moreover, it is not clear to us whether ARM's debugger actually constitutes an external computer. ARM discloses that the debugger is a system that includes a program used to detect, locate, and correct software faults, together with custom hardware that supports software debugging. Glossary-6. However, that disclosure by itself does not indicate that ARM's debugger constitutes an external computer system that receives the highest priority event, as claimed. While ARM's debugger may constitute an

external computer system, we will not resort to such speculation or assumption to cure the deficiency in the factual basis in order to support the Examiner's obviousness rejection. Further, as applied by the Examiner, Dreyer does not remedy the above-noted deficiencies in ARM.

Consequently, the Examiner reliance upon ARM—namely the advanced single core trace and the debugger—does not properly account for the disputed claim limitation. It follows that the Examiner has erred in determining that independent claims 1, 8, and 12 are rendered unpatentable over the combination of ARM and Dreyer.

Claims 2-7 and 9-11

Because dependent claims 2-7 and 9-11 incorporate by reference the same disputed claim limitation as their underlying base claim, the Examiner erred in rejecting these claims for the same reasons set forth in our discussion of independent claims 1, 8, and 12.

IV. CONCLUSIONS

For the foregoing reasons, the Examiner has not erred in rejecting: (1) claims 1-12 as being unpatentable under doctrine of obviousness-type doubling patenting; and (2) claims 1-12 as being unpatentable under 35 U.S.C. § 103(a) over the combination of Swoboda, Dreyer, Izzard, and Swaine. However, the Examiner has erred in rejecting claims 1-12 as being unpatentable under 35 U.S.C. § 103(a) over the combination of ARM and Dreyer.

V. DECISION

We affirm the Examiner's decision to reject: (1) claims 1-12 as being unpatentable under doctrine of obviousness-type doubling patenting; and (2) claims 1-12 as being unpatentable under 35 U.S.C. § 103(a) over the combination of Swoboda, Dreyer, Izzard, and Swaine. However, we reverse the Examiner's decision to reject claims 1-12 as being unpatentable under 35 U.S.C. § 103(a) over the combination of ARM and Dryer.

Because we have affirmed at least one ground of rejection with respect to each claim on appeal, the Examiner's decision is affirmed. *See* 37 C.F.R. § 41.50(a)(1).

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED