



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/100,518	04/07/2005	Hang-Ting Lue	08409.0060	2841
22852	7590	01/31/2013	EXAMINER	
FINNEGAN, HENDERSON, FARABOW, GARRETT & DUNNER LLP 901 NEW YORK AVENUE, NW WASHINGTON, DC 20001-4413			WEISS, HOWARD	
			ART UNIT	PAPER NUMBER
			2814	
			MAIL DATE	DELIVERY MODE
			01/31/2013	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte HANG-TING LUE, MIN-TA WU,
ERH-KUN LAI, YEN-HAO SHIH, CHIA-HUA HO, and
KUANG-YEU HSIEH

Appeal 2010-008510
Application 11/100,518
Technology Center 2800

Before KRISTEN L. DROESCH, JUSTIN BUSCH, and HUNG H. BUI,
Administrative Patent Judges.

BUI, *Administrative Patent Judge.*

DECISION ON APPEAL

Appellants¹ seek our review under 35 U.S.C. § 134(a) of the Examiner's final rejections of claims 1-20 and 37. We have jurisdiction under 35 U.S.C. § 6(b).

We AFFIRM.²

¹ Real Party in Interest is Macronix International Co., Ltd.

² Our decision refers to Appellants' Appeal Brief filed November 5, 2009 ("App. Br."); Reply Brief filed April 26, 2010 ("Reply Br."); Examiner's Answer mailed February 24, 2010; and the original Specification filed April 7, 2005 ("Spec.").

STATEMENT OF THE CASE

Appellants' Invention

Appellants' invention relates to a memory device and, in particular, a "flash memory device that utilizes sub-gates and replaces diffusion regions of the memory cells with inversion regions controlled by the sub-gates." *Spec.* ¶001 and Abstract.

Claims on Appeal

Claim 1 is independent, and is representative of the invention, as reproduced below with disputed limitations emphasized:

1. A semiconductor device, comprising:

a semiconductor substrate, including

a first inversion region,
a second inversion region,
a first diffusion region,
a second diffusion region, and
a channel region between the first inversion region
and the second inversion region;

a word line over the channel region; and

at least one sub-gate over the first and second inversion regions, and at least partially over the first and second diffusion regions;

wherein the word line does not extend over the at least one sub-gate; and

wherein the at least one sub-gate comprises a first sub-gate over the first inversion region and a second sub-gate over the second inversion region.

Evidence Considered

The prior art relied upon by the Examiner in rejecting the claims on appeal is:

Gallagher	U.S. 4,057,820	Nov. 8, 1977
Kamigaki	U.S. 6,674,122 B2	Jan. 6, 2004
Nakamura	U.S. 7,335,937 B2	Feb. 26, 2008

Examiner's Rejections

- (1) Claims 1, 3-9, 11-20, and 37 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Kamigaki and Nakamura. Ans. 3-4.
- (2) Claims 2 and 10 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Kamigaki, Nakamura, and Gallagher. Ans. 5.

*§ 103(a) Rejection of Claims 1, 3-9, 11-20, and 37 over
Kamigaki and Nakamura*

Regarding independent claims 1, 9,³ and 37,⁴ the Examiner finds that Kamigaki teaches or suggests all of the limitations of these claims, except for a word line that is substantially parallel to or does not extend over the at least one sub-gate. Ans. 3-4. The Examiner finds, however, that Nakamura teaches or suggests a word line that is substantially parallel to or does not extend over the at least one sub-gate. Ans. 4. The Examiner concludes that it would have been obvious to combine Kamigaki and Nakamura to achieve high speed reading. *Id.* The Examiner also concludes that a person of ordinary skill in the relevant art would have had a reason to form a word line

³ Independent claim 9 recites similar features of claim 1, including that a word line does not extend over the at least one sub-gate.

⁴ Independent claim 37 recites similar features of claim 1, except that “word lines are substantially parallel with the at least one sub-gate.”

that is substantially parallel to or does not extend over the at least one sub-gate, as disclosed by Nakamura into a flash memory device of Kamigaki “to realize high speed reading.” *Id.*

ISSUE

Based on Appellants’ arguments, the dispositive issue on appeal is whether the Examiner has erred in rejecting claims 1, 3-9, 11-20, and 37 under 35 U.S.C. § 103(a). In particular, the issue turns on whether Kamigaki can be modified to incorporate the teachings of Nakamura in order to arrive at Appellants’ claimed invention without changing the principle of operation of Kamigaki or without rendering Kamigaki inoperable for its intended purpose. App. Br. 11-15; Reply Br. 2-4.

ANALYSIS

We have reviewed the Examiner’s rejections in light of Appellants’ arguments that the Examiner has erred.

We disagree with Appellants’ conclusions as to all rejections. We adopt as our own (1) the findings and reasons set forth by the Examiner in the action from which this appeal is taken and (2) the reasons set forth by the Examiner in the Examiner’s Answer in response to Appellants’ Appeal Brief. We also concur with the conclusions reached by the Examiner, and further highlight and address specific findings and arguments for emphasis as follows.

Independent claims 1, 9, and 37

Appellants contend that if one of ordinary skill in the art were to modify Kamigaki to incorporate the feature of Nakamura as suggested by

the Examiner, the memory cells of the modified Kamigaki would be broken and inoperable. App. Br. 12-13; Reply Br. 2-4. In particular, Appellants argue that:

Kamigaki teaches a multi-storage nonvolatile memory in which a word line (*see, e.g., Kamigaki* at Fig. 16, element 5) extends over at least one sub-gate (*see, e.g., id* at Fig. 16, elements 6-1, 6-2) [and also] teaches, in at least Columns 18 and 19, that the word lines and sub-gates are manufactured in such a way that if the word line did not extend over the sub-gates, connections among the cells in *Kamigaki* would be broken, and the cells in *Kamigaki* would be inoperable (*see, e.g., id.* at col. 19, ll. 4-8, “the electrode material of the memory gate electrode 7 of the memory transistor also serves as the word lines of the memory cell array.”) That is, if one were to modify *Kamigaki* in view of *Nakamura* as suggested... the cells of the modified *Kamigaki* would be broken and inoperable.

App. Br. 12-13. Appellants also argue that:

[i]f one were to “reorient” the word lines in Figure 18 of *Kamigaki* “to that shown in Figure 12 of *Nakamura*” such that the word lines of *Kamigaki* are parallel to bit lines 4Li, 4Lj, and 4Lk of *Kamigaki*, as suggested ..., the reoriented word lines would not cross bit lines 4Li, 4Lj, and 4Lk ... such a hypothetical rearrangement would render the chip inoperable for its intended purpose which includes properly performing write and read operations.

App. Br. 13-14; *see* Reply Br. 3-4.

However, we disagree. At the outset, we note that Appellants’ Specification does not describe or accord any significance of forming a word line that is substantially parallel with the at least one sub-gate (*i.e.*, first and

second sub-gates), or alternatively, a word line that does not extend over at least one sub-gate, as asserted by Appellants.⁵

We also note that:

[T]he test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art.

In re Keller, 642 F.2d 413, 425 (CCPA 1981); *see also In re Sneed*, 710 F.2d 1544, 1550 (Fed. Cir. 1983) (“[I]t is not necessary that the inventions of the references be physically combinable to render obvious the invention under review.”).

Rather, “if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill.” *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 417 (2007). Thus, the Examiner is not simply combining steps or portions of the steps of the methods described by Kamigaki and Nakamura. Instead, the Examiner finds here that, in view of the techniques taught or suggested by Kamigaki and Nakamura, a person of ordinary skill

⁵ Appellants’ Specification only describes that a control gate 514, shown in FIG. 5 (3rd embodiment), is formed over a channel region, between two sub-gates 522 and 524 and, as such, does not extend over the two sub-gates 522 and 524. However, in an effort to distinguish over the Examiner’s rejection of the same claims 1, 3-9, and 11-20 under 35 U.S.C. § 102(b) as being anticipated by Kamigaki, Appellants simply amended the “control gate” as –the word line– in an Amendment filed December 24, 2008. Thus, in the event of further prosecution, we leave it to the Examiner to re-evaluate independent claims 1, 9, and 37 under 35 U.S.C. § 112, ¶1.

in the semiconductor memory art would have had reason to modify the teachings of Kamigaki in a way that would have resulted in Appellants' invention, as recited in claim 1.

Second, we acknowledge that the Examiner's characterization of element "7" as shown in Figures 14 and 15 of Kamigaki as a "word line" is incorrect. Ans. 5. Instead, element 7, shown in Figures 14 and 15 of Kamigaki refers to "a memory gate electrode" disposed between sub-gates 6-1, 6-2. Reply Br. 2. Nevertheless, we agree with the Examiner's findings that the word line(s) of Kamigaki can still be arranged in parallel with at least one sub-gate or not extend over the at least one sub-gate without rendering the memory device of Kamigaki inoperable. Ans. 6. For example, and as correctly found by the Examiner, Figure 27 of Kamigaki shows a memory cell array in which word lines 5L are arranged in parallel with a sub-gate lines 6L and 6La. *Id*; see also Figures 29, 31, and 33 of Kamigaki. This is particularly true as long as the word lines are connected to the control gate and the sub-gates are electrically isolated from the control gate of Kamigaki. See Figure 5 of Kamigaki.

For the reasons set forth above, Appellants have not persuaded us of error in the Examiner's rejection of independent claims 1, 9, and 37 and their respective dependent claims 3-8 and 11-20, which were not separately argued. Accordingly, we sustain the Examiner's rejection of claims 1, 3-9, 11-20, and 37 under 35 U.S.C. § 103(a) as being unpatentable over Kamigaki and Nakamura.

Appeal 2010-008510
Application 11/100,518

CONCLUSION

On the record before us, we conclude that the Examiner has not erred in rejecting claims 1-20 and 37 under 35 U.S.C. § 103(a).

DECISION

As such, we affirm the Examiner's final rejections of claims 1-20 and 37.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv) (2011).

AFFIRMED

ELD