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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte BURKHARD NEURAUTER, HARALD PRETL,
RASTISLAV VAZNY, and THOMAS GREIFENEDER

Appeal 2010-008395
Application 11/704,544
Technology Center 2800

Before, DAVID M. KOHUT, BRYAN F. MOORE, and JOHN G. NEW,
Administrative Patent Judges.

NEW, *Administrative Patent Judge.*

DECISION ON APPEAL

SUMMARY

Appellants file this appeal under 35 U.S.C. § 134(a) from the Examiner's Final Rejection of claims 1-3, 5-9, and 11-21.¹ Specifically, claims 1-3, 5, 6, 9, , 12, 14-15, and 17-21 were rejected by the Examiner as unpatentable under 35 U.S.C. § 103(b) as being anticipated by Yamamoto et al. (Japan Patent No. 2004-140688 A, May 13, 2004) ("Yamamoto"). The Examiner rejected claims 7-8, 11, 13, and 16 as unpatentable under 35 U.S.C. § 103(a) as being obvious over Yamamoto.

We have jurisdiction under 35 U.S.C. § 6(b).

We affirm.

STATEMENT OF THE CASE

Appellants' invention is directed to a loop filter that includes an input terminal, an output terminal, and a control terminal for a selection signal, with at least one low pass filter that is disposed between that input terminal and that output terminal. Abstract.

GROUPING OF CLAIMS

Because Appellants argue that the Examiner erred for substantially the same reason with respect to claims 1, 9, and 14, we select these claims as representative of the claims on appeal. Claim 1 recites:

1. A loop filter, comprising:

an input terminal and an output terminal;

¹ Claims 4 and 10 were previously cancelled and claims 22-28 were withdrawn from consideration. App. Br. 2.

a control terminal configured to receive a selection signal, wherein the loop filter is configured to switch between a first configuration and at least one second configuration in response to the selection signal;

at least one low pass filter disposed between the input terminal and the output terminal; and

a series circuit comprising a switch coupled to the control terminal and a resistor coupled thereto, and a capacitor connected in parallel to the series circuit, wherein the capacitive element is configured to provide an integrating signal transfer characteristics in the second configuration of the loop filter;

wherein in the first configuration the loop filter comprises a non-integrating transfer characteristic in operation and in the second configuration the loop filter comprises an integrating signal transfer characteristic in operation,

wherein the number of poles associated with the loop filter in the first configuration comprising a non-integrating transfer characteristic is non-zero, and the number of poles associated with the loop filter in the second configuration comprising the integrating signal transfer characteristic is greater than the number of poles in the first configuration.

App. Br. 11.

Claim 9 recites:

9. A loop filter, comprising:
 - a signal input terminal and a signal output terminal;
 - a control terminal configured to receive a selection signal;

at least one low pass filter disposed between the signal input terminal and the signal output terminal;

an element comprising an integrating signal transfer characteristic; and

at least one first switch configured to selectively couple the element to the signal input terminal based on a state of the selection signal,

wherein the number of poles associated with the loop filter with the element not coupled to the input terminal is non-zero, and the number of poles associated with the loop filter with the element coupled to the input terminal is greater than the number of poles when the element is not coupled to the input terminal,

wherein the element comprises a parallel circuit comprising a resistor and a capacitor, wherein the resistor is coupled to the signal input terminal via the at least one first switch in a first configuration.

App. Br. 12-13.

Claim 14 recites:

14. A phase locked loop, comprising:

a feedback path;

a phase detector device comprising a reference signal input configured to receive a reference signal and a feedback signal input coupled to the feedback path;

a charge pump comprising an input coupled to an output of the phase detector arrangement;

a loop filter comprising an input coupled to an output of the charge pump, the loop filter comprising a control terminal

configured to receive a selection signal, the loop filter configured to switch between a first configuration and at least one second configuration in response to the selection signal, wherein in the first configuration the loop filter comprises a non-integrating transfer characteristic, and in the second configuration the loop filter comprises an integrating signal transfer characteristic; and

an oscillator device comprising a tuning input terminal and an output, the tuning input terminal coupled to an output of the loop filter, and the output coupled to the feedback path,

wherein the number of poles associated with the loop filter in the first configuration comprising a non-integrating transfer characteristic is non-zero, and the number of poles associated with the loop filter in the second configuration comprising the integrating signal transfer characteristic is greater than the number of poles in the first configuration.

App. Br. 13-14.

ISSUES AND ANALYSES

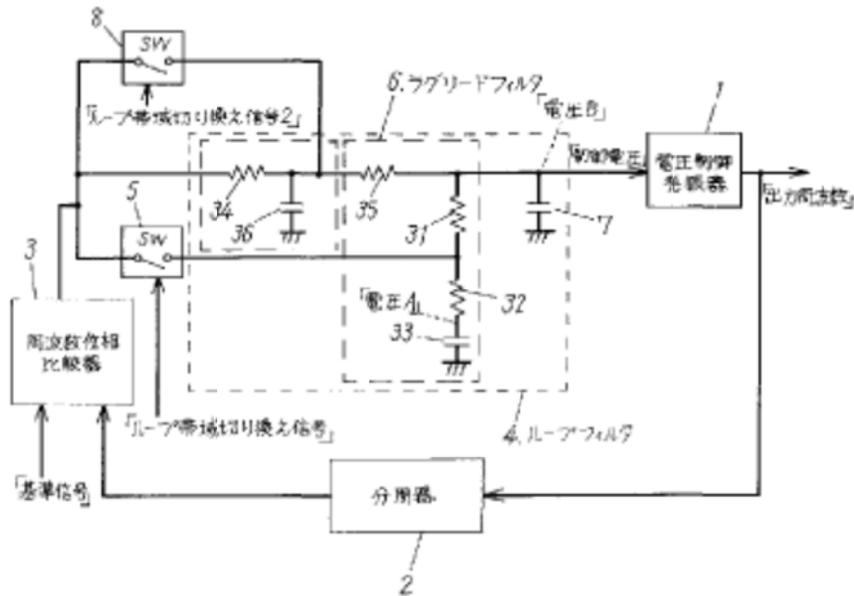
A. Rejection of claim 1

Issue

Appellants argue that the Examiner erred in finding that Yamamoto teaches the limitation of claim 1 reciting a “loop filter comprising a series circuit comprising a switch coupled to the control terminal and a resistor coupled thereto, and a capacitor connected in parallel to the series circuit.” App. Br. 5 (emphasis omitted). We therefore address the issue of whether the Examiner so erred.

Analysis

Appellants argue that Yamamoto fails to teach or suggest “a series circuit comprising a switch coupled to the control terminal and a resistor coupled thereto, and a capacitor connected in parallel to the series circuit.” App. Br. 5 (emphasis omitted). Specifically Appellants contend that Yamamoto teaches a high speed phase-locked loop (PLL) frequency synthesizer comprises a resistor 34 and capacitor 36, and a switch 8 connected in parallel to the resistor 34. *Id.* (citing Yamamoto, Fig. 7, reproduced below).



Yamamoto, Fig. 7 depicts a high speed phase-locked loop (PLL) frequency synthesizer.

Appellants argue that the synthesizer comprises a resistor 34 and capacitor 36, and a switch 8 connected in parallel to the resistor 34. *Id.* Therefore, Appellants contend, Yamamoto discloses that the resistor 34 and switch 8 are in a parallel circuit configuration with respect to each other, in

contrast to claim 1, which recites a resistor and switch in a series circuit configuration and a capacitor in parallel with the resistor and switch. App. Br. 5-6. According to Appellants, elements 8 and 34, are not in a series circuit; rather elements 8 and 34 are in parallel with one another, and consequently do not constitute a series circuit. App. Br. 6.

Appellants further argue that the capacitor 36 is not in parallel with the series circuit as recited in claim 1. *Id.*

The Examiner responds that the circuit that comprises 8 and 31-36 is coupled in series with circuit 3 and also coupled in series with circuit 1. Ans. 6 (*see also* Yamamoto, Fig. 7). The Examiner further finds that the circuit that comprises 8 and 31-36 includes series connected elements [(34, 36) connected in series with 35]. *Id.* Therefore, the Examiner finds, the circuit that comprises 8 and 31-36 can be considered as a series circuit. *Id.*

The Examiner also responds that capacitor 7 has two terminals directly connected to two terminals of the series circuit (8 and 31-36). Therefore, capacitor 7 (and not capacitor 36, as argued by Appellants) is connected in parallel to the series circuit as claimed. *Id.*

We agree with the Examiner. The circuit disclosed in Yamamoto's Fig. 7 is in series with circuits 1 and 3, consequently we find that it is a series circuit as contemplated by the language of the claim. Ans. 6. Moreover, although switch 8 and resistor 34 are in parallel, the language of claim 1 does not require that these individual elements be in series, rather, the disputed limitation requires "a switch coupled to the control terminal and a resistor coupled thereto." Yamamoto's Figure 7 discloses that resistors 34 and 35 are coupled to switch 8, and thereby satisfy the language of the claim. Ans. 6.

Furthermore, we agree with the Examiner that capacitor 7 is in parallel as required by the language of the claim. Ans. 6. We therefore conclude that the Examiner did not err in finding that Yamamoto discloses the limitation of claim 1 reciting a “loop filter comprising a series circuit comprising a switch coupled to the control terminal and a resistor coupled thereto, and a capacitor connected in parallel to the series circuit.”

B. Rejection of claim 9

Issue

Appellants argue that Yamamoto fails to disclose the limitation of claim 9 reciting “wherein the element comprises a parallel circuit comprising a resistor and a capacitor, wherein the resistor is coupled to the signal input terminal via the at least one first switch in a first configuration.” App. Br. 7 (emphasis omitted). We therefore address the issue of whether the Examiner so erred.

Analysis

Appellants reprise their argument, *supra*, that the resistor 34 and the capacitor 36 of Yamamoto are not in parallel, and consequently does not anticipate this claim feature. App. Br. 7. Appellants argue further that when switch 8 is closed, resistor 34 is “shorted out” and is thus bypassed, thereby coupling another resistor 35 to the input terminal (i.e., the output of element 3). *Id.* This, according to Appellants, makes it impossible to satisfy the requirement of claim 9, that resistor 34 be coupled to the signal input terminal via the at least one first switch in a first configuration since the resistor is bypassed in such a configuration. App. Br. 8. Appellants

contend that claim 9 requires a resistor that is coupled to a signal input terminal via (or through) the at least one first switch. *Id.* Consequently, Appellants maintain, the plain meaning of the language of claim 9 requires a switch that is operably coupled between a resistor and a signal input terminal. *Id.* Appellants argue that Yamamoto, by contrast, discloses the resistor 34 is not coupled to the signal input terminal 3 via the at least one first switch 8, rather, resistor 34 is coupled directly to the input terminal 3 and not via the switch 8 as recited in claim 9. *Id.*

In response, the Examiner repeats his finding, *supra*, that capacitor 7 is in parallel with the series circuit (8 and 31-36), and that, therefore, circuit 4 that comprises capacitor 7 in parallel with series circuit (8 and 31-36) can be considered as parallel circuit. Ans. 7.

The Examiner also finds that the parallel circuit comprises resistor (34 or 35) and capacitor (36). *Id.* Resistor 35 is coupled to the input terminal via switch 8. *Id.* The Examiner finds that the second terminal (i.e., the terminal between 34 and 35) of resistor 34 is coupled to the input terminal via switch 8; consequently, resistor 34 is also coupled to the input terminal (at the second terminal) via switch 8. *Id.* The Examiner finds that even if, as Appellants contend, there is a short circuit when switch 8 is closed and there therefore is no current going through resistor 34, the second terminal of resistor 34 is nevertheless still coupled to the input terminal via switch 8. *Id.* Therefore, finds the Examiner, Yamamoto's Fig. 7 discloses an element comprising a parallel circuit (circuit 4) comprising a resistor (34 or 35) and a capacitor (36) wherein the resistor is coupled to the signal input terminal via at least one first switch 8 in a first configuration. *Id.*

We are persuaded by the Examiner's reasoning and adopt it as our own. We have addressed the issue of capacitor 7, *supra*, with respect to claim 1. Moreover, regardless of whether there is current flowing through resistor 34, resistor 34 is nevertheless coupled to switch 8. Consequently, we find that resistor 34 is coupled to switch 8. We consequently find that the Examiner did not err in finding that Yamamoto anticipates the limitations of claim 9.

Claim 14

Issue

Appellants argue that Yamamoto fails to disclose the limitation of claim 14 reciting "a charge pump." App. Br. 8. We therefore address the issue of whether the Examiner so erred.

Analysis

Appellants argue that Yamamoto is silent with respect to a charge pump and that the Examiner erred in finding that a charge pump is inherently disclosed in any phase-locked loop. Appellants contend that "[t]o establish inherency, extrinsic evidence 'must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient.'" App. Br. 9 (emphasis omitted) (quoting MPEP § 2112 (IV); *In re Robertson*, 169 F.3d 743,745 (Fed. Cir.

1999)). Appellants contend that the Examiner has provided no evidentiary support showing that Yamamoto teaches a charge pump. *Id.*

The Examiner responds by adducing Herrmann et al. (US 6,192,094 B1, February 20, 2001) (“Herrmann”) and Kegasa (4,940,952, June 10, 1990) (“Kegasa”). Ans. 7. The Examiner finds that Fig. 2 of Herrmann shows a phase frequency detector, with only one analog output, comprising an internal charge pump 7 that converts the digital signals (UP and DN) outputted from an internal phase frequency detector to an analog signal to be filtered. *Id.* The Examiner also finds that Fig. 4 of Kegasa discloses a phase frequency comparator, which has only one analog output, comprising an internal charge pump (34-39) that converts digital signals outputted from internal phase-frequency comparator to analog signal to be filtered. *Id.* The Examiner therefore finds it is well known in the art that, in a phase-locked loop, a phase frequency detector or comparator that has only one analog, not digital, output must comprise an internal charge pump circuit to convert digital signal outputted from an internal phase-frequency detector to analog signal. *Id.* The Examiner therefore finds that such a charge pump is inherent to claim 14.² *Id.*

We are persuaded by the Examiner’s reasoning and adopt it as our own. Both Herrmann and Kegasa explicitly teach charge pumps as essential components of phase-locked loops in phase-frequency detector and comparator circuits. Ans. 7; *see, e.g.*, Herrmann, col. 1, ll. 6-11; Kegasa, col. 3, ll. 18-34. We therefore conclude that the Examiner did not

² Appellants do not attempt to rebut this evidence in their Reply Brief.

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err in finding that the limitation of claim 14 reciting “a charge pump” is inherent to the invention disclosed by Yamamoto.

DECISION

The Examiner’s rejection of claims 1-3, 5-9, and 11-21 as unpatentable under 35 U.S.C. §102(b) is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED

msc