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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte JOEL HENRY HINRICHS

Appeal 2010-008391
Application 10/999,677
Technology Center 2100

Before DAVID M. KOHUT, BRYAN F. MOORE, and JOHN G. NEW,
Administrative Patent Judges.

NEW, *Administrative Patent Judge.*

DECISION ON APPEAL

SUMMARY

Appellant files this appeal under 35 U.S.C. § 134(a) from the Examiner's Final Rejection of claims 1 and 3-24. Specifically, claims 1, 3, 5, 8, 11, 12, 14-17, and 24 were rejected by the Examiner as unpatentable under 35 U.S.C. § 103(a) as being obvious over the combination of Jarboe, Jr. et al. (US 7,155,637 B2, December 26, 2006) ("Jarboe"), Delcoco et al. (US 5,127,067, June 30, 1992) ("Delcoco"), and Microsoft Corporation, MICROSOFT COMPUTER DICTIONARY 488 (5th ed. 2002) ("Dictionary").

The Examiner rejected claims 4, 7, 9, 10, 18, and 19 as unpatentable under 35 U.S.C. § 103(a) as being obvious over Jarboe, Delcoco, Dictionary, and Chauvel et al. (US 6,684,280 B2, January 27, 2004) ("Chauvel").

The Examiner rejected claims 6 and 13 as being unpatentable under 35 U.S.C. § 103(a) as being obvious over Jarboe, Delcoco, Dictionary, and Arends et al. (US 2003/0140263 A1, July 24, 2003) ("Arends").

The Examiner rejected claim 20 as being unpatentable under 35 U.S.C. § 103(a) as being obvious over Jarboe, Delcoco, Dictionary, and Nguyen et al. (US 6,449,170 B1, September 10, 2002) ("Nguyen").

The Examiner rejected claims 21-23 as being unpatentable under 35 U.S.C. § 103(a) as being obvious over Jarboe, Delcoco, Dictionary, Nguyen, and Arends.

We have jurisdiction under 35 U.S.C. § 6(b).

We reverse.

STATEMENT OF THE CASE

Appellant's invention is directed to a processing system on an integrated circuit includes a group of processing cores. A group of dedicated

random access memories are severally coupled to one of the group of processing cores or shared among the group. A star bus couples the group of processing cores and random. Abstract.

GROUPING OF CLAIMS

Because Appellant argues that the Examiner erred for substantially the same reason with respect to claims 1 and 3-24, we select claim 1 as representative of the claims on appeal. Claim 1 recites:

1. A processing system comprising:
 - a plurality of processing cores on an integrated circuit coupled together; and
 - a plurality of random access memories on the integrated circuit, each of the plurality of random access memories dedicated to one of the plurality of processing cores;
 - wherein a first group of the plurality of processing cores is coupled together for direct communication with one another by a first star bus.

App. Br. 25.

ISSUES AND ANALYSES

A. Rejection of claim 1 under 35 U.S.C. § 103(a)

Issue

Appellant argues that the Examiner erred in rejecting claim 1 as being obvious over Jarboe, Delcoco, and Dictionary. App. Br. 18. Specifically, Appellant argues that the Examiner failed to make a prima facie case that the references, either individually or in combination, fail to teach or suggest the limitations of claim 1. App. Br. 21. We therefore address the issue of whether the Examiner so erred.

Analysis

Appellant admits that Jarboe discloses a data bus (120) through which a data flow control unit (115) can address a plurality of embedded cache memories (110, 111, 112, 113). App. Br. 18. However, Appellant contends, the Examiner failed to show that Jarboe teaches or suggests any manner or any circumstance under which one CPU may communicate with another CPU, either through the data flow control unit or directly with one another as recited in claim 1. *Id.*

Appellant further contends that neither Dictionary nor Delcoco, individually or in combination, remedies this deficiency. App. Br. 18-19. According to Appellant, although Dictionary discloses a general concept of a “system on a chip,” Dictionary does not disclose “a plurality of processing cores coupled together for direct communication with one another by a first star bus.” App. Br. 18. Appellant contends further that Delcoco’s teaching of a LAN is not on an integrated circuit, nor even in a single computer; furthermore, Delcoco also fails to disclose one node in direct communication with another node across a star bus, because its LAN requires protocol communications with, switching by, and transmission through a star network. App. Br. 18-19. Moreover, argues Appellant, the combination of Jarboe, Delcoco, and Dictionary fails to teach or suggest the combination of structure and function recited in claim 1. App. Br. 19. Appellant asserts that since Jarboe and Dictionary do not disclose communication between processor cores, Delcoco must teach or suggest the communication functionality. *Id.* However, Appellant argues, Delcoco does not provide for direct communication between processor cores. *Id.*

Appellant also argues that Jarboe describes problems with “input/output errors and bus conflicts” if each processor core 105, 106, 107, 108 attempts to perform memory tests simultaneously, a problem that is apparently solved by Jarboe’s data flow control unit 115. App. Br. 20 (citing Jarboe, col. 3, ll. 41-52). According to Appellant, adding Delcoco’s LAN between Jarboe’s processor cores would add a separate communications path between the processor cores. App. Br. 20. Appellant asserts that additional communication between processor cores not mediated by Jarboe’s data flow control unit would thus apparently create “input/output errors and bus conflicts” and defeat the intended purpose of Jarboe’s data flow control unit. *Id.*

The Examiner responds that Jarboe teaches a plurality of processing cores coupled together on an integrated circuit. Ans. 9 (citing Jarboe, Fig. 1; Abstract, ll. 2-3; col. 1, ll. 28-30; col. 3, ll. 41-43). The Examiner finds that Delcoco teaches the use of a star bus topology as a way of connecting nodes together. Ans. 9 (citing Delcoco, col. 3, ll. 9-16). The Examiner also finds that Delcoco also teaches that the nodes directly communicate with one another (Ans. 9 (citing col. 3, ll. 33-35 (“[A] star network coupler which directly connect[s] the transmitter of one node to a receiver in only one node”)); *see also* Figs. 1B, 6), and also shows that a transmitter of one node, 52, is directly connected by a switch 54 to a receiver of one node, 50, for the purpose of allowing easy expansion and modification by simply connecting additional nodes to the central hub. Ans. 9.

Furthermore, the Examiner finds that Delcoco discloses a mechanical switch 54 to connect two processor cores and states that “a star network

coupler which directly connect[s] the transmitter of one node to a receiver in only one node.” Ans. 9-10 (quoting Delcoco, Fig. 6; col. 3, ll. 33-35).

We are not persuaded by the Examiner’s reasoning. We find that Jarboe does not teach or suggest core processors in direct communication with each other; rather, Jarboe teaches that each of the core processors on an integrated chip are connected via the bus 120 with the data flow control unit. App. Br. 18; Jarboe, col. 3, ll. 22-25 (“To accomplish this, the data flow control unit 115 is connected to each of the embedded memory caches 110, 111, 112, 113 through a data bus 120.”). Jarboe does not teach or suggest that the individual core processors on an integrated circuit directly communicate with each other; only with the data flow control unit. *Id.*

Neither Dictionary nor Delcoco remedies this deficiency. Dictionary teaches “[a] chip integrating computer, microprocessors, and all necessary support components in a single unit,” but does not teach that the core processors directly communicate with each other. App. Br. 18 (quoting Dictionary 488). Delcoco teaches a LAN, with the various nodes connected via a star bus. App. Br. 18-19. A “node” in a LAN does not generally refer to more than one core processor on an integrated circuit; rather, it is generally used to refer to an end device with a MAC address (typically one for each network interface controller it possesses); examples are computers, packet switches, xDSL modems (with Ethernet interface), and wireless LAN access points on the network. *See, e.g., Node (networking)*, [http://en.wikipedia.org/wiki/Node_\(networking\)](http://en.wikipedia.org/wiki/Node_(networking)). As such, Delcoco does not teach or suggest a plurality of processing cores on an integrated circuit coupled together, and “a plurality of random access memories on the integrated circuit ... wherein a first group of the plurality of processing cores

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is coupled together for direct communication with one another by a first star bus.” We consequently find that the Examiner erred in finding that the combination of Jarboe, Delcoco, and Dictionary teaches or suggests the disputed limitations of claim 1.

B. Rejection of claims 3-24 under 35 U.S.C. § 103(a)

Because we find that the Examiner erred with respect to claim 1, and because Appellant argues, *inter alia*, that claims 3-24 are patentable for the same reasons as claim 1 (App. Br. 21-23), we reverse the Examiner’s rejection of those claims.

DECISION

The Examiner’s rejection of claims 1 and 3-24 as unpatentable under 35 U.S.C. § 103(a) is reversed.

REVERSED

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