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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/331,688	12/30/2002	Samantha J. Edirisooriya	42P15356	3878

7590 01/30/2013
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EXAMINER

FARROKH, HASHEM

ART UNIT	PAPER NUMBER
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2188

MAIL DATE	DELIVERY MODE
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01/30/2013

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte SAMANTHA J. EDIRISOORIYA, SUJAT JAMIL,
DAVID E. MINER, R. FRANK O'BLENESS, STEVEN J. TU,
and HANG T. NGUYEN

Appeal 2010-008290
Application 10/331,688
Technology Center 2100

Before KALYAN K. DESHPANDE, JOHNNY A. KUMAR, and
TREVOR M. JEFFERSON, *Administrative Patent Judges*.

DESHPANDE, *Administrative Patent Judge*.

DECISION ON APPEAL

STATEMENT OF CASE¹

The Appellants seek review under 35 U.S.C. § 134(a) of a Final Rejection of claims 1-4, 6, 18-21, 23, 30-33, 35-39, 43-45, 47, 56, and 59, the only claims pending in the application on appeal. We have jurisdiction over the appeal pursuant to 35 U.S.C. § 6(b).

We AFFIRM.

The Appellants invented multiprocessors that provide hardware cache coherency using shared states. Specification 1:2-5.

An understanding of the invention can be derived from a reading of exemplary claim 1, which is reproduced below [bracketed matter and some paragraphing added]:

1. A method comprising:

- [1] enabling a processor cache to receive a request to push data into the processor cache by a non-processor agent; and
- [2] ensuring coherency between caches of at least two different processors.

REFERENCES

The Examiner relies on the following prior art:

Duncan	US 6,353,877 B1	Mar. 5, 2002
Chen et al.	2002/0166031 A1	Nov. 7, 2002

¹ Our decision will make reference to the Appellants' Appeal Brief ("App. Br.," filed Feb. 18, 2010) the Examiner's Answer ("Ans.," mailed Aug. 19, 2009), and Final Rejection ("Final Rej.," mailed Nov. 30, 2005).

REJECTIONS²

Claims 1, 4, 35, 43, 56, and 59 stand rejected under 35 U.S.C. §102(e) as being anticipated by Duncan.

Claims 1-3, 6, 35-36, 38-39, 43-45, 47, 52, and 54 stand rejected under 35 U.S.C. §102(e) as being anticipated by Chen.

Claims 37 and 53 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Duncan and Chen.

ISSUES

The issue of whether the Examiner erred in rejecting claims 1, 4, 35, 43, 56, and 59 under 35 U.S.C. § 102(e) as being anticipated by Duncan turns on whether Duncan describes “enabling a processor cache to receive a request to push data into the processor cache by a non-processor agent.”

The issue of whether the Examiner erred in rejecting claims 1-3, 6, 35-36, 38-39, 43-45, 47, 52, and 54 under 35 U.S.C. § 102(e) as being anticipated by Chen turns on whether Chen describes “enabling a processor cache to receive a request to push data into the processor cache by a non-processor agent.”

The issue of whether the Examiner erred in rejecting claims 37 and 53 under 35 U.S.C. § 103(a) as unpatentable over Chen and Duncan turns on whether the Appellants’ arguments in support of claim 1 are found to be persuasive.

² Claims 5, 7-17, 22, 24-29, 34, 40-42, 46, 48-51, 55, 57, 58, 60, and 61 are objected to as being dependent upon rejected base claims. Final Rej. 10-11.

ANALYSIS

We have reviewed the Examiner's rejections in light of the Appellants' contentions that the Examiner has erred.

We disagree with the Appellants' conclusions. We adopt as our own (1) the findings and reasons set forth by the Examiner in the action from which this appeal is taken and (2) the reasons set forth by the Examiner in the Examiner's Answer in response to the Appellants' Appeal Brief. We concur with the conclusion reached by the Examiner. We highlight the following arguments for emphasis.

Claims 1, 4, 35, 43, 56, and 59 rejected under 35 U.S.C. §102(e) as being anticipated by Duncan

The Appellants contend that Duncan fails to describe "enabling a processor cache to receive a request to push data into the processor cache by a non-processor agent," as recited by claims 1 and 4 and as similarly recited by claims 35, 43, 56, and 59. App. Br. 5-10.

We disagree with the Appellants. As found by the Examiner, Duncan describes a plurality of cacheable devices and a plurality of non-cacheable devices coupled on a bus. Ans. 6 (citing Duncan 3:2-14). Duncan further describes that the I/O device will modify the cache and subsequently modify the main memory. Ans. 14 (citing Duncan 8:41-44). That is, Duncan describes a processor that receives a write request to write to cache.

The Appellants acknowledge this teaching by Duncan and argue that "Duncan appears to be reducing the number of transactions issued on the bus by issuing a single transaction to the main memory such that the subsequent

aligned byte blocks are written.” (emphasis in original) App. Br. 7. However, this argument does not persuade us of error on part of the Examiner because the Appellants’ argument does not distinguish the claimed invention from Duncan. The Appellants’ argument merely asserts possible features of Duncan, but do not rebut the Examiner’s findings in the disclosure of Duncan that describes the claimed invention. Accordingly, we do not find the Appellants’ arguments persuasive.

Claims 1-3, 6, 35-36, 38-39, 43-45, 47, 52, and 54 rejected under 35 U.S.C. §102(e) as being anticipated by Chen

The Appellants contend that Chen fails to describe “enabling a processor cache to receive a request to push data into the processor cache by a non-processor agent,” as recited by claims 1-3 and 6 and as similarly recited by claims 35-36, 38-39, 43-45, 47, 52, and 54. App. Br. 10-13.

We disagree with the Appellants. The Appellants specifically argue that Chen describes a file cache, but there is no indication that the file cache is a processor cache. App. Br. 11. However, we are not persuaded by this argument. As found by the Examiner, Chen describes that each node comprises a processor and an amount of cache. Ans. 12 (citing Chen ¶ 0024 and Fig. 1). That is, this cache memory is associated with the processor of that node. As such, we do not find the Appellants’ argument to be persuasive.

We are also not persuaded by the Appellants’ argument that the host or host storage area of Chen may not comprise a non-processor agent. App. Br. 11-12. The Examiner found that the Specification of the claimed invention illustrates that a “non-processor agent” encompasses wireless

interfaces. Specification 8:12-16. The Examiner further finds non-processor agents, such as wireless interfaces, encompass host end interfaces, as described by Chen. Ans. 12 (citing Chen ¶ 0024). The Appellants have failed to provide any persuasive evidence or rationale to rebut these findings by the Examiner. Accordingly, we sustain the Examiner's rejection.

*Claims 37 and 53 rejected under 35 U.S.C. §103(a) as being unpatentable
over Duncan and Chen*

The Appellants contend that claims 37 and 53 depend from claims 35 and 43 and the Examiner erred in rejecting claims 37 and 53 for the same reasons asserted in support of claims 35 and 43. We disagree with the Appellants. The Appellants' arguments in support of claims 35 and 43 were not found to be persuasive *supra* and are not persuasive here for the same reasons.

CONCLUSIONS

The Examiner did not err in rejecting claims 1, 4, 35, 43, 56, and 59 under 35 U.S.C. § 102(e) as being anticipated by Duncan.

The Examiner did not err in rejecting claims 1-3, 6, 35-36, 38-39, 43-45, 47, 52, and 54 under 35 U.S.C. § 102(e) as being anticipated by Chen.

The Examiner did not err in rejecting claims 37 and 53 under 35 U.S.C. § 103(a) as unpatentable over Chen and Duncan.

DECISION

To summarize, our decision is as follows.

Appeal 2010-008290
Application 10/331,688

- The rejection of claims 1, 4, 35, 43, 56, and 59 under 35 U.S.C. § 102(e) as being anticipated by Duncan is sustained.
- The rejection of claims 1-3, 6, 35-36, 38-39, 43-45, 47, 52, and 54 under 35 U.S.C. § 102(e) as being anticipated by Chen is sustained.
- The rejection of claims 37 and 53 under 35 U.S.C. § 103(a) as unpatentable over Chen and Duncan is sustained.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED

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