



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

Table with 5 columns: APPLICATION NO., FILING DATE, FIRST NAMED INVENTOR, ATTORNEY DOCKET NO., CONFIRMATION NO. Includes application details for 11/186,515 and 22879, inventor Dacheng (Henry) Zhou, and examiner MALEK, LEILA.

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

JERRY.SHORMA@HP.COM
ipa.mail@hp.com
brandon.serwan@hp.com

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte DACHENG (HENRY) ZOHOU

Appeal 2010-008161
Application 11/186,515
Technology Center 2600

Before ALLEN R. MacDONALD, ROBERT E. NAPPI, and
GEORGIANNA W. BRADEN, *Administrative Patent Judges*.

BRADEN, *Administrative Patent Judges*.

DECISION ON APPEAL

This is an appeal¹ under 35 U.S.C. § 134(a) from a Final Rejection of claims 1-37. We have jurisdiction under 35 U.S.C. § 6(b).

We affirm.

STATEMENT OF THE CASE

Appellants' invention relates to a data clock recovery system for a communication system. (Abstract.)

Claim 1 is exemplary and reproduced below, with disputed limitation in italics:

1. A data clock recovery system, comprising:
 - a phase detector configured to produce a first signal indicating whether a data clock lags or leads a preferred phase in relation to an input data stream; and
 - a phase controller configured to process the first signal to update a phase of the data clock toward the preferred phase such that *the number of incremental changes of phase for each update varies depending on a length of time the data clock lags or leads the preferred phase.*

REJECTIONS

Claims 1, 7, 8, 10, 11, 13, 14, 20, 21, 23, 24, 26, 27, 32-35, and 37 stand rejected under 35 U.S.C. § 102(a) as anticipated by Appellant's Background information in the application's Specification.

Claims 12, 25, and 36 stand rejected under 35 U.S.C. § 103(a) as obvious over Appellant's Background information in the application's Specification.

¹ The Real Party in Interest is Hewlett-Packard Development Company, LP.

ISSUE

Appellant argues that the prior art system fails to disclose specifically that the number of incremental changes of phase for each update varies depending on a length of time the data clock lags or leads the preferred phase. (App. Br. 4.)

Issue: Has the Examiner erred in finding that the prior art system discloses the limitation “the number of incremental changes of phase for each update varies depending on a length of time the data clock lags or leads the preferred phase” as recited in claim 1?

ANALYSIS

We review the Examiner’s rejections in light of Appellant’s arguments that the Examiner has erred. We are unpersuaded by Appellant’s argument (App. Br. 4) that the prior art system does not render anticipate independent claim 1, which recites the limitation “the number of incremental changes of phase for each update varies depending on a length of time the data clock lags or leads the preferred phase.”

The Appellant contends that “the phase count determines when the phase is updated, not the number of incremental changes of phase for each update.” (App. Br. 4-5, emphasis in original.) However, as the Examiner noted (Ans. 7), for each bit period (or clock cycle) in which the data clock 112 of the prior art system lags its preferred phase, the counter 104 increments the phase count 120 by one. “Due to the lack of any further details in the claim for limitation ‘number of incremental changes of phase,’ Examiner gives this limitation, its broadest reasonable interpretation.” (Ans. 7.) Therefore, the Examiner finds the prior art system corresponds to the recited claim limitation. We agree with the Examiner.

Appellant further contends that

in the prior art system the phase is updated by the output of the threshold comparator 106. When the phase count exceeds a threshold value, then the phase is updated by the threshold comparator, by generating a single pulse that either advances the phase or delays the phase by one incremental shift. That is, in the prior art, for each update, the number of incremental changes of phase is a constant, not a variable number as specified in claims 1, 14, and 27. (App. Br. 4 (emphasis in original); Reply Br. 4-6.)

Appellant concludes that “the counter and phase count signal do not determine the number of incremental changes of phase specified in claims 1 and 14.” (App. Br. 5, emphasis in original; Reply Br. 4-6.) However, the Examiner finds the prior art system discloses

that for each bit period in which the data clock lags its preferred phase, the counter 104 increments the phase count by one.” For instance, in one update, if the number of LAGs is equal to two, the value of the phase counter will be two. However, if there are more LAGs in the next cycle, the counter will show a different number. Therefore, the number of incremental changes of phase is not necessarily a constant number in the prior art and depends on the number of detected LAGs. (Ans. 8; the prior art system paragraph [0009], Fig. 3.).

In the Reply Brief, the Appellant argues that “[e]ven if the counter 104 can be incremented by greater than the value one in some conditions, that does not change the fact that once the counter 104 reaches the threshold value (*e.g.*, 64), only **one** pulse on the phase shift signal 122 is generated, which causes a change of phase by just **one phase of the interpolated**

phases of the phase interpolator 108-a constant adjustment.” (Reply Br. 4 (emphasis in original).) Appellant appears to dismiss the aspect of the prior art system where if “the data clock 112 still lags its preferred phase, as indicated by the phase difference signal 118 from the data sampler 102, the counter 104 increments the phase count 120 once per bit period from zero past the threshold.” (See the prior art system paragraph [0009].) Therefore, the Examiner properly finds “the number of incremental changes of phase is not necessarily a constant number in the prior art.” (Ans. 8; the prior art system paragraph [0009], Fig. 3.). Thus, we agree with the Examiner’s findings and conclusions.

Accordingly, we sustain the rejection of independent claim 1 under 35 U.S.C. § 102(a).

Independent claims 14 and 27 recite limitations similar to those discussed with respect to independent claim 1, and Appellant does not present any additional substantive arguments with respect to these claims. Therefore, we sustain the rejections of claims 14 and 27. Further, Appellant does not present any additional substantive arguments with respect to dependent claims 7, 8, 10, 11-13, 20, 21, 23-26, and 32- 37. We sustain the rejection of claims 7, 8, 10, 11-13, 20, 21, 23-26, and 32- 37.

DECISION

The Examiner’s decision to reject claims 1-37 is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED

Vsh