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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte GURTEJ S. SANDHU and D. MARK DURCAN

Appeal 2010-007682
Application 11/185,186
Technology Center 2800

Before MARC S. HOFF, CARLA M. KRIVAK, and
ELENI MANTIS MERCADER, *Administrative Patent Judges*.

MANTIS MERCADER, *Administrative Patent Judge*.

DECISION ON APPEAL

STATEMENT OF THE CASE

Appellants appeal under 35 U.S.C. § 134(a) from a final rejection of claims 41-49, 51, 52, 54, 55, 57-62, 64-68, and 70-76. We have jurisdiction under 35 U.S.C. § 6(b).

We affirm-in-part.

THE INVENTION

Appellants' claimed invention is directed to a semiconductor substrate and a trench extending into the substrate. The trench has a narrow bottom portion and an upper wide portion over the bottom portion and joining to the bottom portion at a step. A substantially solid electrically insulative material substantially fills the trench. A void can be within the substantially solid insulative material, and at least substantially entirely within the bottom portion of the trench. Spec. ¶ [0006].

Independent claim 41, reproduced below, is representative of the subject matter on appeal.

41. A method of forming a semiconductor construction, comprising:
 - providing a semiconductor substrate;
 - forming a first opening extending into the substrate, the first opening having a first width;
 - forming a second opening extending downwardly into the substrate from the first opening, the second opening having a second width which is less than the first width;
 - forming electrically insulative material within the first and second openings, the electrically insulative material substantially filling the first opening and leaving a void within the second opening;
 - and
 - out-gassing material from the insulative material into the void.

REFERENCES and REJECTIONS

1. The Examiner rejected claim 71 under 35 U.S.C. § 112, first paragraph, as lacking enablement.
2. The Examiner rejected claims 41-44, 51, 52, 62, 64, 70, and 72 under 35 U.S.C. § 102(b) as anticipated by Hong (Sug Hun Hong et al., *A Novel T-Shaped Shallow Trench Isolation Technology*, 40 JAPAN J. APPLIED PHYSICS 2616 (2001)) as evidenced by Subramanian (US 6,445,072 B2; Sept. 3, 2002) and Horie (US 5,928,428; July 27, 1999).
3. The Examiner rejected claims 58-61 under 35 U.S.C. § 102(b) as anticipated by Sridhar (US 5,930,595; July 27, 1999) as evidenced by Subramanian and Horie.
4. The Examiner rejected claims 45, 65-68, and 76 under 35 U.S.C. § 103(a) as obvious over Hong and Kameyama (US 4,472,240; Sept. 18, 1984).
5. The Examiner rejected claims 46, 48, 49, 54, 55, 57, and 71 under 35 U.S.C. § 103(a) as obvious over Hong and Sandhu (US 2004/0224510 A1; Nov. 11, 2004).
6. The Examiner rejected claim 47 under 35 U.S.C. § 103(a) as obvious over Hong, Sandhu, and Kim (US 6,620,681 B1; Sept. 16, 2003).
7. The Examiner rejected claim 73 under 35 U.S.C. § 103(a) as obvious over Hong and Price (US 4,639,288; Jan. 27, 1987).
8. The Examiner rejected claim 74 under 35 U.S.C. § 103(a) as obvious over Hong and Tang (US 6,727,150 B2; Apr. 27, 2004).
9. The Examiner rejected claim 75 under 35 U.S.C. § 103(a) as obvious over Hong, Sandhu, and Tang.

ISSUES

The issues are whether the Examiner erred in finding that:

1. Claim 71 lacks enablement;
2. Hong as evidenced by Subramanian and Horie teaches “out-gassing material from the insulative material into the void” as recited in claim 41;
3. Hong as evidenced by Subramanian and Horie teaches “a plurality of steps in the semiconductor substrate” as recited in claim 62;
4. Sridhar as evidenced by Subramanian and Horie teaches “forming a void in the first material; and providing a second material into the void” as recited in claim 58; and
5. Hong in combination with Sandhu teaches the limitation of “filling the upper portions of the openings and leaving voids within the lower portions of the openings, the electrically insulative material comprising at least gelatinous material” as recited in claim 46;
6. Hong in combination with Kameyama teaches “after the removing of the mask and while the uppermost surface of the semiconductor substrate is devoid of material, providing a material into the trench” as recited in claim 65.

PRINCIPLES OF LAW

The claims, of course, do not stand alone. Rather, they are part of “a fully integrated written instrument” consisting principally of a specification that concludes with the claims. For that reason, claims “must be read in view of the specification, of which they are a part.” . . . [T]he specification “is always highly relevant to the claim construction analysis.

Usually, it is dispositive; it is the single best guide to the meaning of a disputed term.”

Phillips v. AWH Corp., 415 F.3d 1303, 1315 (Fed. Cir. 2005) (citations omitted).

To establish inherency, the extrinsic evidence ““must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill.”” *In re Robertson*, 169 F.3d 743, 745 (Fed. Cir. 1999) (citation omitted).

The Supreme Court stated that “[r]ejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.”” *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007) (quoting *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006)).

ANALYSIS

1. Does claim 71 lack enablement?

Appellants assert that the Examiner failed to provide a minimal requirement of giving a reason of the uncertainty of the enablement of the terms “forming right angle corners” in substrates without undue experimentation (App. Br. 7).

We do not agree. The Examiner acknowledged that the drawings show steps formed in right angles (Ans. 4). However, doubt may arise about enablement because information is missing about one or more essential parts or relationships between parts which one skilled in the art could not develop without undue experimentation. In such a case, the Examiner should specifically identify what information is missing and why one skilled in the

art could not supply the information without undue experimentation. *See* MPEP § 2164.06(a).

The Examiner identified what information is missing by stating that the Specification fails to teach one having ordinary skill in the art by what method the right angle steps are formed and omitting any detail as to how to form the intersection of the upper and lower portions to form right angles (Ans. 4). The Examiner further noted that based on the prosecution history it did not appear that a method such as anisotropic etching could form such right angles (Ans. 17), thus indicating that one skilled in the art could not supply the information without undue experimentation. Accordingly, the Examiner did satisfy the minimal requirement of giving a reason for the uncertainty of the enablement of “forming right angle corners” in substrates without undue experimentation.

Accordingly, we affirm the Examiner’s rejection of claim 71 under 35 U.S.C. § 112, first paragraph, as lacking enablement.

2. Claims 41-45, 51, 52, 70, and 74

Appellants argue that Hong as evidenced by Subramanian and Horie do not teach “out-gassing material from the insulative material into the void” as recited in claim 41 (App. Br. 8-10).

We agree with Appellants’ argument. The Examiner relies on Hong for the creation of a “void” (Ans. 19). The Examiner then relies on Horie (col. 2, ll. 24-32) for teaching out-gassing during the formation of silicon oxide films (Ans. 19). The Examiner also relies on Subramanian (col. 5, ll. 5-25) for teaching material trapped within the void wherein the contents are primarily determined by the atmosphere in which the preliminary gap fill dielectric layer is formed (Ans. 19). The Examiner concludes that in light of

Horie's and Subramanian's teaching, those skilled in the semiconductor art would have easily concluded that the void of Hong, similar to the void of Subramanian, inherently contains the out-gassing material from the insulative material (*id.*).

Appellants rebut by stating that Specification paragraph [0048] discloses that a particular gas within the voids can be the ambient present during deposition of insulative material 40 "or"¹ gases formed by out-gassing from insulative material 40 (Reply Br. 4). Appellants note that one is clearly distinctive from the other, and therefore a teaching to one is not a teaching to the other (*id.*). In other words, Subramanian's teaching (col. 5, ll. 5-25) of material being trapped within the void wherein the contents are primarily determined by *the atmosphere* in which the preliminary gap fill dielectric layer is formed (Ans. 19) does not satisfy the claim limitation which requires that the outgassing material is *from the insulative material and not the atmosphere* (*see* Reply Br. 4).

Accordingly, we reverse the Examiner's rejection of claim 41 and for the same reasons the rejections of claims 42-45, 51, 52, 70, and 74.

3. Claims 62, 64, 72, and 73

Appellants argue that Hong as evidenced by Subramanian and Horie does not teach a "trench comprising a plurality of steps in the semiconductor substrate" because Hong teaches a single step extending into a semiconductor substrate (App. Br. 14-15).

¹ The Specification actually states "and/or" instead of just "or" as argued by Appellants, but nonetheless there is a clear disclosure of the alternative "or" and Appellants have claimed the alternative embodiment in claim 41.

We do not agree with Appellants' arguments. We turn to Appellants' Specification for the definition of a "semiconductor substrate" because the Specification is the single best guide to the meaning of a disputed term. *See Phillips*, 415 F.3d at 1315.

Appellants' Specification defines the "semiconductor substrate" to mean "any construction comprising semiconductive material, including, but not limited to, bulk semiconductive materials such as a semiconductive wafer (either alone or in assemblies comprising other materials thereon)" (§ [0037]). Accordingly, Hong's assembly of SiN layer, poly-Si Layer, and a pad oxide layer on the silicon substrate constitutes a "semiconductor substrate" consistent with the Specification. Furthermore, the trench comprising a plurality of steps in the "semiconductor substrate" as shown in Hong's Figure 2 satisfies the disputed limitation of a "trench comprising a plurality of steps in the semiconductor substrate" as recited in claim 62.

Accordingly, we affirm the Examiner's rejection of claim 62 and for the same reasons the Examiner's rejections of dependent claims 64, 72, and 73 which were not separately argued.

4. Claims 58-61

Appellants argue that Sridhar as evidenced by Subramanian and Horie do not teach "forming a void in the first material; and providing a second material into the void" as recited in claim 58 (App. Br. 15).

We agree with Appellants that Sridhar teaches an *unfilled* tubular volume 109 in an oxide 108 (col. 3, ll. 30-39) and the Examiner relied on the *unfilled* tubular volume 109 to teach a void (App. Br. 15-16). Accordingly, we agree with Appellants that the collective teachings of the references demonstrate that the missing descriptive matter (filling the void/tubular

volume) is not *necessarily* present in the Sridhar processing reference as Sridhar clearly teaches the contrary (*see* App. Br. 16). *See Robertson*, 169 F.3d at 745.

Thus, we reverse the Examiner’s rejection of claim 58 and for the same reasons the rejection of claims 59-61.

5. Claims 46, 48, 49, 54, 55, 57, 71, and 75

Appellants argue that Hong in combination with Sandhu does not teach the limitation of “filling the upper portions of the openings and leaving voids within the lower portions of the openings, the electrically insulative material comprising at least gelatinous material” as recited in claim 46.

We agree with Appellants’ argument. Sandhu teaches away from the creation of voids and uses the sol gel to avoid “undesirable voids” (*see* Sandhu ¶ [0007]). Accordingly, the combination does not reasonably teach filling the voids with gelatinous material.

Accordingly, we reverse the Examiner’s rejection of claim 46 and the rejections of claims 48, 49, 54, 55, 57, 71, and 75 for the same reasons.

6. Claims 65-68 and 76

Appellants argue that the rationale articulated by the Examiner of modifying Hong in view of Kameyama “so that the surface of the insulating film becomes flat” does not provide a rational underpinning to support the legal conclusion of obviousness (App. Br. 22-23 (citation omitted) (emphasis omitted)).

We agree with Appellants’ argument. The Supreme Court stated that “[r]ejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning

with some rational underpinning to support the legal conclusion of obviousness.” *See KSR*, 550 U.S. at 418 (citation omitted).

The Examiner states Kameyama (col. 1, ll. 30-35) teaches that when the groove is filled by an insulating film it results in an insulating film that is flat (Ans. 24-25). While the reference does teach a resulting flat film, the Examiner has not articulated why a skilled artisan would want to modify Hong with this teaching, or why the resulting flat film would be a desirable modification. Accordingly, the Examiner did not provide a rational underpinning to support the legal conclusion of obviousness.

Accordingly, we reverse the Examiner’s rejection of claim 65 and for the same reasons the rejection of claims 66-68 and 76.

CONCLUSIONS

The Examiner did not err in finding that:

1. Claim 71 lacks enablement; and
2. Hong as evidenced by Subramanian and Horie teaches “a plurality of steps in the semiconductor substrate” as recited in claim 62.

The Examiner erred in finding that:

3. Sridhar as evidenced by Subramanian and Horie teaches “forming a void in the first material; and providing a second material into the void” as recited in claim 58;
4. Hong as evidenced by Subramanian and Horie teaches “out-gassing material from the insulative material into the void” as recited in claim 41;
5. Hong in combination with Sandhu teaches the limitation of “filling the upper portions of the openings and leaving voids within the

- lower portions of the openings, the electrically insulative material comprising at least gelatinous material” as recited in claim 46; and
6. Hong in combination with Kameyama teaches “after the removing of the mask and while the uppermost surface of the semiconductor substrate is devoid of material, providing a material into the trench” as recited in claim 65.

DECISION

The Examiner’s decision rejecting claim 71 under 35 U.S.C. § 112 is affirmed. The Examiner’s decision rejecting claims 62, 64, 72, and 73 is affirmed. The Examiner’s decision rejecting claims 41-45, 46-49, 51, 52, 54, 55, 57, 58-61, 65-68, 70, 71, 74, 75 and 76 is reversed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED-IN-PART

babc