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Table with 5 columns: APPLICATION NO., FILING DATE, FIRST NAMED INVENTOR, ATTORNEY DOCKET NO., CONFIRMATION NO. Includes application details for William P. Tsu and examination information for Examiner TSENG, CHENG YUAN.

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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*Ex parte* WILLIAM P. TSU

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Appeal 2010-005987  
Application 11/253,870  
Technology Center 3900

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Before, ERIC S. FRAHM, DAVID M. KOHUT, and  
JOHN G. NEW, *Administrative Patent Judges*.

KOHUT, *Administrative Patent Judge*.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134(a) of the Final Rejection of claims 1-3, 8-10, 12-14, 20, and 22-32.<sup>1</sup> We have jurisdiction under 35 U.S.C. § 6(b).

We affirm-in-part the Examiner's rejection of these claims.

## INVENTION

The invention is directed to a system and method for encoding a packet header to enable higher bandwidth efficiency across Peripheral Component Interconnect Express links. Spec. 2. Claim 1 is representative of the invention and is reproduced below:

1. In a computer system having a first device and a second device coupled to each other by a bus link, a method of processing a memory read request by the second device, the method comprising the steps of:
  - a. generating the memory read request including a completion tag by the first device, the completion tag indexing a tracking table that is stored in the first device;
  - b. transmitting the memory read request over the bus link from the first device to the second device to issue the memory read request;
  - c. receiving the memory read request issued by the first device over the bus link;
  - d. reading data from a memory location in accordance with the memory read request;
  - e. generating a read completion packet including a header portion including a Transaction Layer Packet sequence number and the completion tag, wherein the completion tag is used by the first device to recover a requisite parameter associated with the memory read request and the recovered requisite parameter is not transmitted in the read completion packet; and
  - f. transmitting the read completion packet, included in a Data Link Layer Header (DLLH) together with at least four

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<sup>1</sup> Claims 4-7, 11, 15-19, and 21 were previously cancelled.

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bytes of Link Cyclic Redundant Check (LCRC) code, over the bus link to the first device to allow the first device to recover the requisite parameter from the tracking table.

## REFERENCES

Birdwell                      US 6,032,197                      Feb. 29, 2000

PCI Express Base Specification Revision 1.1 (March 28, 2005). PCI-SIG.<sup>2</sup>

## REJECTION AT ISSUE

Claims 1-3, 8-10, 12-14, 20, and 22-32 are rejected under 35 U.S.C. § 103(a) as being unpatentable over PCIe and Birdwell. Ans. 3-12.

## ISSUES

Did the Examiner err in finding that the combination of PCIe and Birdwell teaches or suggests generating a memory read request including a completion tag that indexes a tracking table, as required in claims 1 and 14?

Did the Examiner err in finding that the combination of PCIe and Birdwell teaches or suggests that certain bits within a header portion are assumed to have a value of zero and that other bits are assumed to have a value of one, as required in claim 8?

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<sup>2</sup> Hereinafter referred to as PCIe.

## ANALYSIS

### *Claims 1-3, 14, 20, and 22-32*

Independent claim 1 recites “generating the memory read request including a completion tag by the first device, the completion tag indexing a tracking table that is stored in the first device”. Independent claim 14 contains a similar limitation. Claims 2-3 and 22-29 are dependent upon independent claim 1; claims 20 and 30-32 are dependent upon independent claim 14. The Examiner finds that PCIe teaches a reserved field that can be defined to include a completion tag. Ans. 4-7 and 14. Appellant argues that the Examiner’s finding is in error because PCIe states that “all TLP fields marked Reserved . . . must be filled with all 0’s when a TLP is formed.” App. Br. 13 (emphasis in original); PCIe pg. 47. We further note that the definition of “reserve” in PCIe cited by the Examiner states that “Reserved register fields must be read only and must return 0 when read.” Ans. 13; PCIe pg. 24. We agree with Appellant. The Examiner has not cited to any portion of the reference, nor do we find anywhere in the reference, where it is taught that the reserved field can be anything other than 0. Therefore, the Examiner has failed to show that the reserved field of PCIe is capable of being defined to include a completion tag indexing a tracking table, as required by claim 1. Thus, for the reasons stated *supra*, we cannot sustain the Examiner’s rejection of claims 1-3, 14, 20, and 22-32.

### *Claims 8-10 and 12-13*

We select claim 8 as representative of the group of claims comprising 8-10 and 12-13 as Appellant has not argued any of the other claims with particularity. 37 C.F.R. § 41.37(c)(1)(vii). Claim 8 recites:

. . . transmitting the memory write request packet over the bus link to the second device, wherein a third bit of the TC field, which is

assumed to be zero, a TD field, which is assumed to be zero, an EP field, which is assumed to be zero, each of a last DW BE field and a first DW BE field, which are both assumed to have a value of one, and a requester ID and a memory-write tag are not included in header portion and are not transmitted.

(Claim 8). Appellant argues that neither PCIe nor Birdwell teach that any bits in the header field are assumed to have a value of zero or one because Birdwell does not assume the values of any of the fields as the values are stored in the header table. App. Br. 16-17; Reply Br. 6-7.

First, we note that claims are interpreted broadly and a broad interpretation of the claim term “assumed to be zero” does not require the field to be zero. Second, the Examiner finds that there is a finite number of identified, predictable solutions (i.e. values of fields in digital communications being “only Z, 0, or 1.”) Ans. 7-8. Appellant has not addressed the Examiner’s specific finding and thus, we agree with the Examiner. Therefore, since the values of the fields are either Z, 0, or 1, it is reasonable to assume that the value of a field is either Z, 0, or 1, which encompasses the claimed “assumed to be zero” limitation recited in claim 8. As a result, we agree with the Examiner (Ans. 10-11) that PCIe teaches a TC field (pg. 64), TD field (pg. 55), and EP fields (pg. 55) assumed to have a value of 0, and DW BE fields having a value of one (pg. 55).

For the reasons discussed *supra*, we sustain the Examiner’s rejection of claim 8 and claims 9-10 and 12-13 that have been grouped with claim 8.

## CONCLUSIONS

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The Examiner erred in finding that the combination of PCIe and Birdwell teaches or suggests generating a memory read request including a completion tag that indexes a tracking table, as required in claims 1 and 14.

The Examiner did not err in finding that the combination of PCIe and Birdwell teaches or suggests that certain bits within a header portion are assumed to be zero and that other bits are assumed to have a value of one, as required in claim 8.

#### SUMMARY

The Examiner's decision to reject claims 1-3, 14, 20, and 22-32 is reversed.

The Examiner's decision to reject claims 8-10 and 12-13 is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED-IN-PART

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