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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte HIROKI FUJISAWA

Appeal 2010-005492
Application 11/522,424
Technology Center 2100

Before DENISE M. POTHIER, ERIC B. CHEN, and
STANLEY M. WEINBERG, *Administrative Patent Judges*.

WEINBERG, *Administrative Patent Judge*.

DECISION ON APPEAL

Appellant appeals under 35 U.S.C. § 134(a) from the Examiner's rejection of claims 1-9, 11-18, and 20. We have jurisdiction under 35 U.S.C. § 6(b).

We affirm-in-part.

Claims 1-9 and 11-17 stand rejected under 35 U.S.C. § 103(a) as obvious over Matano (US 5,949,734; Sept. 7, 1999) in view of Abbiate (US 2002/0070761 A1; June 13, 2002).[1]

Claims 18 and 20 stand rejected under 35 U.S.C. § 103(a) as obvious over Matano in view of Suzuki (US 4,138,732; Feb. 6, 1979).

Although claim 19 was appealed (Br. 2), the Examiner subsequently allowed it. Ans. 18.

Claim 10 has been canceled.[2]

STATEMENT OF THE CASE

Appellant's invention determines when data transfer (read or write) has been completed so that power-down can commence. When multiple transfer (read or write) operations have occurred, the invention uses two counters to maintain a history of the data transfer commands and issues a completion signal when all of the transfers have been completed so that power-down can be effected. The history and completion functions are maintained by using two counters. The first counter counts the number of read or write instructions (i.e., maintains a history of the number of instructions). The second counter counts the number of read or write

[1] Throughout this opinion, we refer to (1) the Appeal Brief filed September 8, 2009; and (2) the Examiner's Answer mailed December 8, 2009.
[2] Although the Examiner addresses claim 10 in the rejection (Ans.3, 9), this claim has been canceled and will not be further discussed. Br. 2.

completions. When all of the read or write instructions have been completed, the count values are equal and power-down begins. *See* Spec. 1, 6, 9, 24-26; Fig. 6.

Independent claim 1 is illustrative with key disputed limitations emphasized:

> 1. A data transfer operation completion detection circuit that is used in a semiconductor device that can transfer data in response to each of data transfer commands and can *accept a new one of the data transfer commands while a data transfer operation sequence corresponding to a previous one of the data transfer commands, is in progress*, comprising:
>
> a first circuit that responds to each of the data transfer commands and *maintains a reception history indicative of at least the number of the data transfer commands whose data transfer operation sequences have not been yet completed*; and
>
> a second circuit that *generates a data transfer completion signal when the data transfer operation sequences have been performed the number of times corresponding to the number of the data transfer commands indicated by the reception history*.

THE OBVIOUSNESS REJECTION OVER MATANO AND ABBIATE

The Examiner finds that Matano teaches every recited feature of claim 1 except for (1) a device that "accept[s] a new one of the data transfer commands while a data transfer operation sequence corresponding to a previous one of the data transfer commands is in progress;" and (2) "a first circuit that responds to each of the data transfer commands and maintains a reception history indicative of at least the number of the data transfer commands whose data transfer operation sequences have not been yet completed." Ans. 4. The Examiner further finds that Abbiate teaches the limitations missing from Matano and concludes that it would have been obvious to modify Matano using Abbiate's teachings. Ans. 4-6.

Appellant argues that a combination of Matano and Abbiate does not teach or suggest accepting data transfer commands while a data transfer operation sequence corresponding to a previous one of the data transfer commands is in progress (Br. 7); maintaining a reception history indicative of at least the number of the data transfer commands whose data transfer operation sequences have not been yet completed (Br. 7:10-12, 15-18; 8:2-5, 15-17); and generating a data transfer completion signal when the data transfer operation sequences have been performed the number of time corresponding to the number of the data transfer commands indicated by the reception history (Br. 7:15-16, 18-20; 8:15-16, 18-20).

ISSUES

Under § 103, has the Examiner erred in rejecting claim 1 by finding that the combination of Matano and Abbiate teaches:

(1) a data transfer operation completion detection circuit that accepts a new one of the data transfer commands while a data transfer operation sequence corresponding to a previous one of the data transfer commands is in progress?

(2) a first circuit that maintains a reception history indicative of at least the number of the data transfer commands whose data transfer operation sequences have not been yet completed?

(3) a second circuit that generates a data transfer completion signal when the data transfer operation sequences have been performed the number of time corresponding to the number of the data transfer commands indicated by the reception history?

FINDINGS OF FACT

1. Matano teaches a semiconductor device that can transfer data by reading memory information from a memory block (col. 3, ll. 14-18) in response to data transfer commands (e.g., COMMAND in Fig. 1). Col. 6, ll. 20-22. The device has a circuit 6 (mapped to the claimed second circuit at Ans. 3-4) that generates a data transfer completion signal and informs a CPU of completion of data read for all target memory blocks. Fig. 1; col. 6, ll. 29-32.

2. Abbiate's device has a first clock that controls a first counter 100-1 so that the counter content is incremented at each pulse of the first clock; and a second clock that similarly controls a second counter 100-2. Fig. 1; ¶¶ 0009, 0021. In one embodiment, when the frequencies of the two clocks are different, the counters are equal after several clock pulses resulting in the output of comparator 110 changing to a value of 1. Fig. 3; ¶ 0024.

ANALYSIS

Claims 1-9 and 11-15

The Examiner finds that when Abbiate's first counter increases after each pulse of the first clock, this action is analogous to the claimed accepts a new data transfer command while a data transfer operation sequence corresponding to a previous one of the data transfer commands is in progress. Ans. 4:13-18. The Examiner also finds that Abbiate's second counter is analogous to the claimed generates a data transfer completion signal. Ans. 4:20-21. FF 2.

The Examiner therefore finds that the teachings of Abbiate's Figure 3 can be applied to Matano so that Abbiate's first counter would increment

every time a transfer command is received (instead of a clock pulse) and that a second counter would increment every time a transfer is completed. Ans. 4:15-21. The Examiner also finds that because Abbiate's first counter applied to Matano would increment every time a transfer command is received, the counter would maintain a reception history because it would represent the number of transfer commands received and also the number of data transfer commands whose data transfer operation sequences have not yet been completed. Ans. 5:2-7; 19:3-5, 17-21.

The Examiner concludes that it would have been obvious to incorporate the Abbiate teachings into Matano because Abbiate teaches a way of detecting when two counters are equal. The detection of data transfer completion would occur in Matano when the number of commands received equals the number of commands performed. Ans. 5:18-19; 5:22–6:1. *See also* FF 1.

Appellant presents three types ofarguments, none of which are persuasive. The first type of argument contends the references individually. Br. 7:7-12, 15-20. But, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. *See In re Keller*, 642 F.2d 413, 426 (CCPA 1981); *In re Merck & Co., Inc.*, 800 F.2d 1091, 1097 (Fed. Cir. 1986).

The second type of argument recites Appellant's claim language. Br. 7:8-12, 16-20; 8:3-7, 16-20. Such arguments are not persuasive. *See* 37 C.F.R. § 41.37(c)(1)(vii) (noting that an argument that merely points out what a claim recites is unpersuasive). *Accord In re Lovin*, 652 F.3d 1349, 1357 (Fed. Cir. 2011) ("[T]he Board reasonably interpreted Rule 41.37 to require more substantive arguments in an appeal brief than a mere recitation

of the claim elements and a naked assertion that the corresponding elements were not found in the prior art.”).

For the third type ofargument, Appellant contends that although Abbiate teaches that content of a counter is modified after each supplied pulse, such a teaching is not sufficient to suggest modification of Matano to arrive at the claimed invention as a whole. Br. 8:1-3. This argument is not persuasive because it does not provide an adequate explanation that rebuts the Examiner’s specific findings and conclusions. *Compare with* Ans. 4:19–5:7, 18-22; 6:1-5.

We are therefore not persuaded that the Examiner erred in rejecting (1) representative claim 1; and (2) claims 2-9 and 11-15 not separately argued with particularity, beyond reciting their respective claim language. Br. 10-12. *See In re Lovin, supra*.

Accordingly, we will sustain the Examiner’s rejection of claims 1-9 and 11-15.

Claims 16 and 17

The Examiner provides detailed reasons why the combination of Matano and Abbiate teaches the limitations of claim 16. Ans. 11-13, 20. Appellant’s arguments are not persuasive because they recite various limitations of claim 16. Br. 9:15-19, 21-23; 10:8-10. *See In re Lovin, supra*. In addition, Appellant argues that even if Matano were modified in view of Abbiate’s teaching of counters performing shifting operations, “the claimed invention, as a whole, would not result.” (Br. 10:5-6. The argument is not persuasive because it does not provide an adequate explanation that rebuts the Examiner’s specific findings and conclusions. *Compare with* Ans. 11-13, 20.

We are therefore not persuaded that the Examiner erred in rejecting (1) representative claim 16; and (2) claim 17 not separately argued with particularity.

Accordingly, we will sustain the Examiner's rejection of claims 16 and 17.

THE OBVIOUSNESS REJECTION OVER MATANO AND SUZUKI

Claims 18 and 20

We do not, however, sustain the Examiner's rejection of claims 18 and 20 reciting a counter circuit that indicates the number of unfinished data transfer operations being zero (claim 18) and a counter that counts up and down to indicate data transfer initiation and completion (claim 20).

Referring to claim 18, the Examiner finds that Matano teaches a counter 4 (Ans. 15:2-3, 5). The Examiner also finds that Suzuki teaches a counter circuit (up/down counter 38) that indicates a number of unfinished data transfer operations and the number of unfinished data transfer operations being zero. Ans. 14:19–15:1. The Examiner concludes that in view of Suzuki, it would have been obvious that "the counter of Matano '734 can be an up/down counter that counts up every time a transfer command is received and counts down every time a read/write transfer is completed." Ans. 15:5-8. As a result, the Examiner concludes, "[w]hen the up/down counter is at zero, it is an indication that all transfer commands received have been completed." Ans. 15:8-9. According to the Examiner, using an up/down counter as taught by Suzuki would be "merely utilizing an alternative type of counter to produce similar results." Ans. 15:17-18.

The Examiner further finds that Matano's block count memory means 4 counts the number of blocks that are to be transferred and Matano's data transfer completion means 6 counts the number of blocks that have been transferred. Ans. 22:3-6. The Examiner concludes that it would have been obvious to replace Matano's transfer block count memory means 4 and its data transfer completion means 6 with Suzuki's up/down counter. Ans. 21:20-21.

With the above-described substitutions, the Examiner concludes that the up/down counter would count up every time a transfer block to be transferred is received and count down every time the transfer block is transferred. Ans. 22:10-11. "Essentially, one up/down counter would be replacing two counters and a comparator. It would be obvious to do so since they produce the same results, i.e. the determination of when all pending data transfers have been completed." Ans. 22:13-16.

Appellant contends that instead of using a counter circuit to indicate a number of unfinished data transfer operations, Matano compares a predetermined value stored in its element 4 with a value of an internal counter included in its element 6 in response to the output from its element 5. That is, element 6 only detects whether its count value reaches a predetermined value. Br. 12:20–13:2. Consequently, Matano's operation is based on interaction between its elements 4, 5, and 6. Br. 13:18-19.

Appellant also contends that Suzuki does not suggest generating a completion detection signal when the number of unfinished operations is zero (Br. 15:8-12) because Suzuki's up/down counter does not reach zero when the number of transferred blocks equals the number of data blocks to be transferred. Br. 15:13-15.

We agree with Appellant.

Matano teaches only one counter – its element 6. Col. 7, ll. 60-61. Although element 4 stores the *number* of transfer or memory blocks subjected to a data read/write (col. 6, ll. 20-24; col. 7, ll. 37-43, 62-63), there is no indication in Matano that its element 4 acts as a counter that can increase its count once the transferred number is stored there. In addition, Matano's element 6 provides a data transfer completion signal when the value in element 6 equals the value in element 4 based upon a *comparison* of the two values. Col. 7, l. 60–col. 8, l. 3. As Appellant points out, Matano teaches "comparing a fixed value with a variable value." Br. 17:3. Accordingly, contrary to the Examiner's finding, Matano does not teach two counters and a comparator. Ans. 13:14.

In addition, although Suzuki uses two counters 38, 39 that are identified as up/down counters, the counters do not count both upward *and* downward as part of a single operation and do not indicate completion of data transfer by counting down to zero. *See* col. 2, ll. 51-54 (indicating the counter counts up *or* down). Instead, when the count value of counter 38, for example, reaches the last designated address A_k, "no count clock signal CLK1 is generated and the output instruction of the program disappears. Consequently, the counter 38 is stopped at the count value A_k." Col. 3, ll. 25-29. That is, counter 38 indicates completion of data transfer by stopping at the end of its upward count, not by counting to zero, such that a detection circuit generates a signal in response to the counter indicating the unfinished data transfer operations being zero as recited in claim 18.

Accordingly, the Examiner has also failed to prove by a preponderance of the evidence that it would have been obvious to use an

up/down counter that counts up every time a transfer is received, counts down every time a read/write transfer is completed, and uses a zero indication on the up/down counter to indicate that all transfer commands received have been completed as recited in independent claim 20.

We are therefore constrained by the record before us to find that the Examiner erred in rejecting claim 18 and claim 20 for similar reasons.

Accordingly, we will not sustain the Examiner's rejection of claims 18 and 20.

CONCLUSION

Under § 103, the Examiner did not err in rejecting claims 1-9 and 11-17, but did err in rejecting claims 18 and 20.

DECISION

The Examiner's decision rejecting claims 1-9 and 11-17 is affirmed. The Examiner's decision rejecting claims 18 and 20 is reversed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1). *See* 37 C.F.R. § 1.136(a)(1)(iv) (2010).

AFFIRMED-IN-PART

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