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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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*Ex parte* RAJINDER P. SINGH, MURALIDHARAN S.  
CHINNAKONDA, and BHASI KAITHAMANA

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Appeal 2010-004116  
Application 11/060,142  
Technology Center 2100

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Before JOSEPH F. RUGGIERO, BRADLEY W. BAUMEISTER, and  
JENNIFER S. BISK, *Administrative Patent Judges*.

BISK, *Administrative Patent Judge*.

DECISION ON APPEAL

## SUMMARY

This is an appeal under 35 U.S.C. § 134(a) from the Examiner's rejection of claims 1-3, 5-11, and 13-18. Claims 4 and 12 have been canceled. Br. 5. We have jurisdiction under 35 U.S.C. § 6(b).

We affirm.

### *The Invention*

The claims are directed to data alignment and sign extension in a processor. Abstract. Specifically, the claims require arranging data bytes from a cache onto a data bus of size greater or equal to 64 bits and also performing a sign extension on the data bus within a single clock cycle. Claim 1, reproduced below with emphasis added, is illustrative of the claimed subject matter.

1. A method comprising:

loading a plurality of data bytes from a data cache in response to a load instruction;

using a first logic, determining the most significant bit of at least one of the data bytes;

using a second logic coupled to the first logic, *arranging at least some of the data bytes onto a data bus in a single clock cycle, the data bus's size greater or equal to 64 bits; and*

*using the second logic, performing a sign extension on the data bus on less than 64 bits of data within said single clock cycle.*

### *The Rejections*

1. Claims 1, 5-9, 11, 13, and 14 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Greenley (US 5,761,469; June 2, 1998). Ans. 4-10.

2. Claims 2 and 3 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Greenley and Patterson (JOHN L. HENNESSY & DAVID A. PATTERSON, *COMPUTER ARCHITECTURE: A QUANTITATIVE APPROACH* 187 (3d ed. 2002)). Ans. 10-11.
3. Claims 10 and 15-18 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Greenley and Official Notice. Ans. 11-13.

### ISSUE

Under § 103, has the Examiner erred in rejecting claim 1 by finding that, in view of the teachings of Greenley, a person of ordinary skill in the art would have found it obvious to slow down the clock and perform both the data alignment and sign extension steps disclosed in Greenley in one clock cycle?

### ANALYSIS

#### *Rejection #1*

The Examiner finds that Greenley teaches every limitation of independent claim 1. Ans. 14. Specifically, the Examiner finds that Greenley expressly teaches that in older generation processors data alignment and sign extension is completed in one clock cycle. Ans. 14 (citing Greenley col. 3, ll. 17-19). According to the Examiner, Greenley also teaches that modern 64-bit processors, with faster clock speeds and clock cycles of approximately six nanoseconds, may require two clock cycles to complete both the data and sign extensions. Ans. 14-15 (citing Greenley col. 3, ll. 23-26); *also see* Ans. 5-6. The Examiner also finds that Greenley details the disadvantages of requiring extra clock cycles. Ans. 15; *see* Greenley col. 3, ll. 41-63. Thus, the Examiner concludes that a person of

ordinary skill would have found it obvious, based on the teachings of Greenley, to slow the clock speed of a 64-bit processor and perform both steps in one clock cycle. Ans. 7, 15.

Appellants do not explicitly dispute any of the Examiner's factual findings. Instead, Appellants assert that the Examiner erred in finding claim 1 obvious over Greenley because Greenley fails to teach or suggest "arranging at least some of the data bytes onto a data bus in a single clock cycle, the data bus's size greater or equal to 64 bits; and using the second logic, performing a sign extension on the data bus on less than 64 bits of data within said single clock cycle." Br. 10-11 (internal quotation marks omitted). Appellants make three arguments to support this assertion.

First, Appellants argue, citing language describing one embodiment of Greenley's invention, that Greenley teaches away from the quoted limitation. Br. 11. Appellants quote the following language from Greenley: (1) "signed opcode LOAD instructions, the processor's pipelines are scheduled to execute opcode signed LOAD instructions in two clock cycle regardless of whether the data accessed is positive or negative" (col. 4, ll. 17-20); and (2) "[t]he inability to perform data alignment and sign extension in one cycle means that 64-bit processors supporting load alignments and sign extensions may have to take additional cycle time to perform a LOAD from memory" (*id.* at 3, ll. 41-44).

We do not agree with Appellants that this language teaches away from slowing the clock speed and performing both data alignment and sign extension in one clock cycle. Instead, it simply supports the Examiner's finding that in a particular embodiment of Greenley, which uses a 64-bit processor with a very high clock speed; the two steps must be performed in

more than one clock cycle. Given the fact that Greenley teaches that one clock cycle completion is preferable and can be done with lower clock speeds, we find reasonable the Examiner's conclusion that a person skilled in the art would have been motivated to modify Greenley in precisely this manner. The mere fact that Greenley teaches using two clock cycles to complete the steps as a preferred embodiment does not constitute "teaching away" from other reasonable uses of the invention. *See Pregis Corp. v. Kappos*, 2012 WL 6051956 at \*5 (Fed. Cir. Dec. 6, 2012).

Second, Appellants argue that the Examiner erred by not relying "on official notice of facts or common knowledge under MPEP 2144.03 to support the bare assertion of obviousness over portions of the claims Examiner notes that Greenley does not teach." Br. 12. We are not persuaded by this argument. The Examiner properly pointed to language in Greenley teaching both that data alignment and sign extension can be done in one clock cycle at slower clock speeds and that there are advantages to doing so. Ans. 4-5 (citing Greenley col. 3, ll. 25-27 and 38-40); 14-15 (citing Greenley col. 3, ll. 17-19 and 23-26). For the same reasons, we are not persuaded by Appellants' third argument—that the Examiner used improper hindsight.

In summary, we are not persuaded of error in the Examiner's rejection of claim 1 as obvious over Greenley. Appellants rely on the same arguments to argue that independent claims 6 and 11 and dependent claims 5, 7-9, 13, and 14 are patentable. Ans. 10-12. Thus, we affirm the Examiner's rejection of claims 1, 5-9, 11, 13, and 14.

*Rejection #2*

Appellants rely on the arguments made with respect to claim 1 for the separate obviousness rejection of claims 2 and 3. Br. 12. For the reasons discussed above, we sustain the rejections of claims 2 and 3.

*Rejection #3*

Appellants rely on the arguments made with respect to claim 1 for the separate obviousness rejection of claims 10 and 15-18. Br. 12. For the reasons discussed above, we sustain the rejections of claims 10 and 15-18.

DECISION

The Examiner's decision rejecting claims 1-3, 5-11, and 13-18 is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED

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