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Gregory W. Osterloth Holland & Hart, LLP P.O. Box 8749 Denver, CO 80201			CHUNG, PHUNG M	
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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte REID HAYHOW

Appeal 2010-000308
Application 10/666,024
Technology Center 2100

Before MARC S. HOFF, CARLA M. KRIVAK, and
CARL W. WHITEHEAD, JR., *Administrative Patent Judges*.

KRIVAK, *Administrative Patent Judge*.

DECISION ON APPEAL

Appellant appeals under 35 U.S.C. § 134(a) from a non-final rejection of claims 1-16. We have jurisdiction under 35 U.S.C. § 6(b).

We affirm.

STATEMENT OF THE CASE

Appellant's claimed invention is directed to methods and systems for determining memory requirements for device testing. That is, required memory needed to execute a plurality of test vectors is determined. (Spec. ¶ [0005]).

Independent claim 1, reproduced below, is representative of the subject matter on appeal.

1. A method comprising:

reading a test file including a plurality of test vectors to be applied to a device; and

determining a required memory needed to execute the plurality of test vectors.

REFERENCES and REJECTION

The Examiner rejected claims 1-16 under 35 U.S.C. § 103(a) based upon the teachings of Hughes (US Patent No. 4,493,079, Aug. 18, 1982) and Regelman (US Patent No. 6,574,626 B1, June 03, 2003).

ANALYSIS

Claims 1, 7-10, 14, and 15

The Examiner finds Hughes discloses the limitations of claim 1 except for determining a required memory to execute a plurality of test vectors and cites Regelman for disclosing this feature (Ans. 3-4). The Examiner asserts Regelman allocates space in a primary memory for called patterns and

dependencies and also determines if there is sufficient room in a primary memory to copy additional software units (*id.*).

Appellant contends the Examiner is incorrect in finding the combination of Hughes and Regelman teaches or suggests Appellant's invention. That is, Appellant asserts the Examiner is correct Hughes does not determine a required memory to execute a plurality of test vectors, but Regelman does not cure this deficiency. (App. Br. 8-9). Appellant contends, Regelman uses a brute force approach that requires a tester be equipped with a significant amount of memory to store all the test vectors and to merely increase the amount of memory in the SRAM to accommodate the entire test program, rather than determining how much memory to add or what happens if there is not enough memory, as claimed (App. Br. 9).

First, it should be noted Appellant's claims only recite "determining a required memory needed to execute the plurality of test vectors." The claims do not set forth how this determination occurs. Further, we agree with the Examiner that Appellant's arguments regarding Regelman failing to "indicate how one determines how much memory to add, or what happens if there is not enough memory" (App. Br. 9; Reply Br. 3) are not commensurate in scope with Appellant's broad claim language (Ans. 10). Rather, Appellant appears to be reading limitations from the Specification into the claims. Further, not only do Appellant's claims not set forth how the amount of memory required is determined, Appellant admits Regelman "could certainly be modified to implement the method of claim 1" (App. Br. 9). In light of Appellant's admission, the Examiner's findings and the broad claim scope, we are not persuaded of Examiner error and find the weight of the evidence supports the Examiner's ultimate legal conclusion of

obviousness (*see* Ans. 9-10). Therefore we sustain the Examiner's rejection of claim 1 and claims 7-10, 14, and 15 dependent therefrom (App. Br. 10).

Claims 2-6, 11-13, and 16

With respect to claims 2-4 and 11-13, Appellant contends Regelman does not teach the step of determining the required memory and that an integrated circuit wafer of Regelman is not the same as a "board of a tester" as recited in claim 2 (App. Br. 10-11). Appellant further argues Regelman does not teach determining the required memory (Ans. 10).

The Examiner disagrees with Appellant and finds Hughes discloses a test system to test integrated circuit boards, referred to as "incircuit" testers and Regelman discloses determining a required memory needed for test points/channels (plurality of pins) of a tester (Ans. 13). Appellant does not contest these findings. Rather, Appellant asserts an "integrated circuit wafer *might* be a 'device' to which vectors are applied" (emphasis added) (App. Br. 11). We agree with the Examiner's findings and find the weight of the evidence supports the Examiner's ultimate legal conclusion of obviousness (Ans.13-14). Therefore we sustain the Examiner's rejection of claim 2 and claims 3, 4, and 11-13.

With respect to claim 5, Appellant asserts nowhere does Regelman disclose the limitations of claim 5 and further, Regelman does not "teach that the amount of memory required 'to execute a plurality of test vectors' is determined" (App. Br. 11-12). Appellant, however, provide no adequate quantitative measurement of the amount of memory required nor substantive arguments as to why Regelman does not teach this amount other than to conclude it is so. *See In re Geisler*, 116 F.3d 1465, 1470 (Fed. Cir. 1997)

(attorney arguments or conclusory statements are insufficient to rebut a prima facie case).

We are therefore not persuaded of Examiner error and find the weight of the evidence supports the Examiner's ultimate legal conclusion of obviousness (*see* Ans. 14-15). The Examiner's rejection of claims 5 and 6, argued together, is sustained.

Claim 16

Appellant essentially provides the same argument with respect to claim 16 as to claim 1: Regelman does not disclose a required memory (App. Br. 12). Appellant further asserts the Examiner has not provided any evidence to support the finding that it would have been obvious to bill a user for required memory (*id.*).

It is noted that claim 16 does not recite *how* the required memory bills a customer. The Examiner has provided a reasonable scenario that is not precluded by the breadth of claim 16 (Ans. 7-8; 16-17). Thus, we are not persuaded of Examiner error and find the weight of the evidence supports the Examiner's ultimate legal conclusion of obviousness.

DECISION

The Examiner's decision rejecting claims 1-16 is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED

Vsh